

SPDT SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

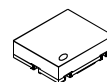
The NJG1660HA8 is a GaAs SPDT switch IC suited for antenna switch of WiMAX application and other wireless handsets.

The NJG1660HA8 features high power handling, low insertion loss, high isolation and wide frequency coverage up to 8.0GHz.

The NJG1660HA8 has ESD protection circuit for good ESD tolerance.

An ultra- small and ultra-thin package of USB6-A8 is adopted.

■ PACKAGE OUTLINE



NJG1660HA8

■ APPLICATIONS

WiMAX, WLAN applications

Mobile phone, Tablet PC, Data card and others wireless handset applications

Antenna switching, path switching, band switching applications

■ FEATURES

● Low insertion loss

0.35dB typ. @f=2.5GHz, $P_{IN}=25\text{dBm}$

0.45dB typ. @f=3.5GHz, $P_{IN}=25\text{dBm}$

0.50dB typ. @f=6.0GHz, $P_{IN}=25\text{dBm}$

● High isolation

33dB typ. @f=2.5GHz, $P_{IN}=25\text{dBm}$

30dB typ. @f=3.5GHz, $P_{IN}=25\text{dBm}$

21dB typ. @f=6.0GHz, $P_{IN}=25\text{dBm}$

● Input power at 0.1dB compression point

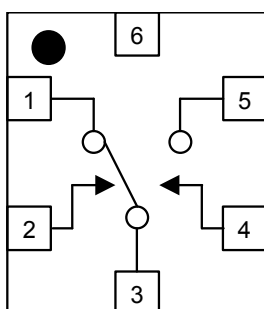
$P_{-0.1\text{dB}}=30\text{dBm min. @f=2.5GHz/3.5GHz, } V_{CTL(H)}=3.0\text{V}$

● Package

USB6-A8 (Package size: 1.0 x 1.2 x 0.38mm typ.)

■ PIN CONFIGURATION

(Top view)



Pin Connection

1. P2
2. CTL2
3. PC
4. CTL1
5. P1
6. GND

■ TRUTH TABLE

"H"= $V_{CTL(H)}$, "L"= $V_{CTL(L)}$		
PATH	CTL1	CTL2
PC-P1	H	L
PC-P2	L	H

NOTE: The information on this datasheet is subject to change without notice

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NJG1660HA8

■ ABSOLUTE MAXIMUM RATINGS

$T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\text{ ohm}$

PARAMETER	SYMBOL	CONDITIONS	CONDITIONS	UNITS
RF Input power	P_{IN}	$V_{CTL}=0/3.0\text{V}$	32	dBm
Control voltage	V_{CTL}	CTL terminal	6.0	V
Power dissipation	P_D	On PCB Board, $T_{jmax}=150^{\circ}\text{C}$	150	mW
Operating temp.	T_{opr}		$-40\sim+85$	$^{\circ}\text{C}$
Storage temp.	T_{stg}		$-55\sim+150$	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS

General conditions: $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=3.0\text{V}$, $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\text{ ohm}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Control voltage (High)	$V_{CTL(L)}$		-0.3	-	0.3	V
Control voltage (Low)	$V_{CTL(H)}$		2.0	3.0	5.0	V
Control current	I_{CTL}		-	5	10	μA
Insertion loss 1	LOSS1	$f=2.5\text{GHz}$, $P_{IN}=25\text{dBm}$	-	0.35	0.55	dB
Insertion loss 2	LOSS2	$f=3.5\text{GHz}$, $P_{IN}=25\text{dBm}$	-	0.45	0.60	dB
Insertion loss 3	LOSS3	$f=6.0\text{GHz}$, $P_{IN}=25\text{dBm}$	-	0.50	0.65	dB
Isolation 1	ISL1	$f=2.5\text{GHz}$, $P_{IN}=25\text{dBm}$	30	33	-	dB
Isolation 2	ISL2	$f=3.5\text{GHz}$, $P_{IN}=25\text{dBm}$	27	30	-	dB
Isolation 3	ISL3	$f=6.0\text{GHz}$, $P_{IN}=25\text{dBm}$	18	21	-	dB
Input power at 0.1dB compression point 1	$P_{-0.1\text{dB}(1)}$	$f=2.5\text{GHz}$	30	-	-	dBm
Input power at 0.1dB compression point 2	$P_{-0.1\text{dB}(2)}$	$f=3.5\text{GHz}$	30	-	-	dBm
VSWR	VSWR	$f=3.5\text{GHz}$, ON STATE	-	1.2	1.4	-
Switching time	T_{SW}	50% V_{CTL} to 10/90% RF	-	150	300	ns

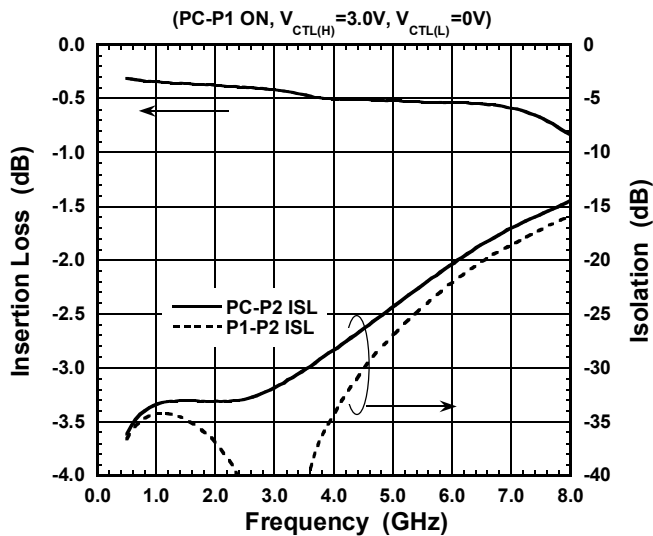
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■ TERMINAL INFORMATION

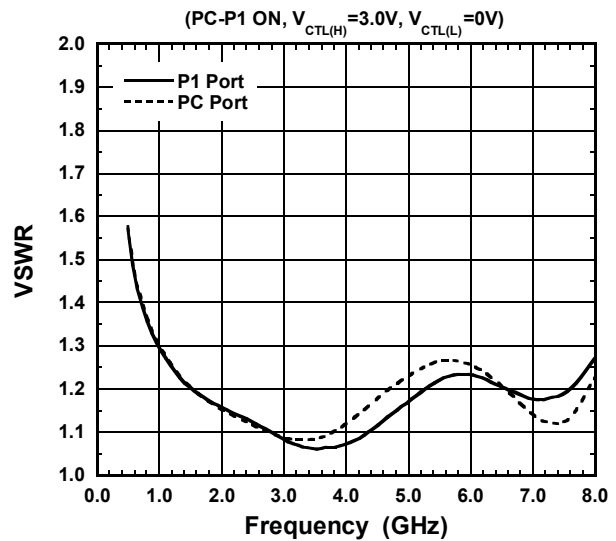
No.	SYMBOL	DESCRIPTION
1	P2	RF port. This port is connected with PC port by controlling 2nd pin to $V_{CTL(H)}$ and 4th pin to $V_{CTL(L)}$. External capacitors are required to block the DC bias voltage of internal circuit.
2	CTL2	Control signal input terminal. Please connect a bypass capacitor (10pF) with a ground plane for avoiding RF noise from outside.
3	PC	Common RF port. External capacitors are required to block the DC bias voltage of internal circuit.
4	CTL1	Control signal input terminal. Please connect a bypass capacitor (10pF) with a ground plane for avoiding RF noise from outside.
5	P1	RF port. This port is connected with PC port by controlling 2nd pin to $V_{CTL(L)}$ and 4th pin to $V_{CTL(H)}$. External capacitors are required to block the DC bias voltage of internal circuit.
6	GND	Ground terminal. Please connect this terminal with a ground plane as close as possible for good RF performance.

■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

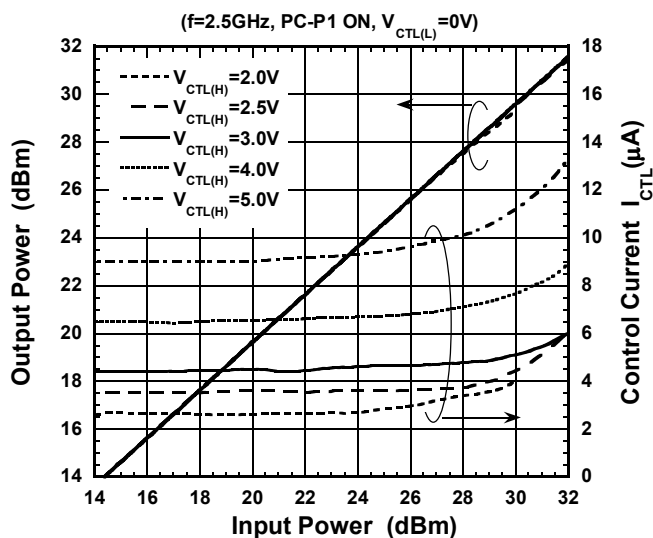
Loss, ISL vs Frequency



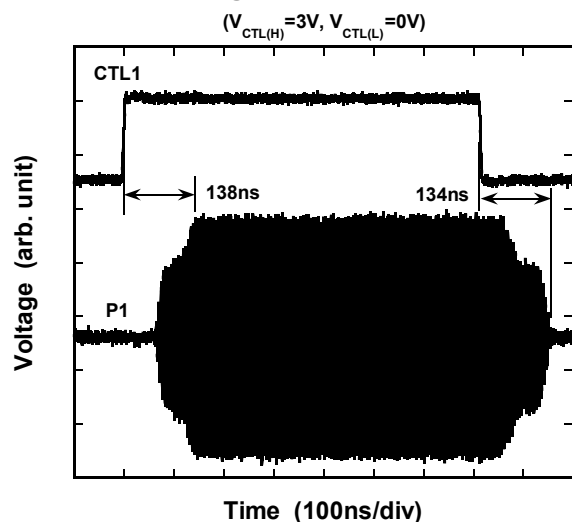
VSWR vs Frequency



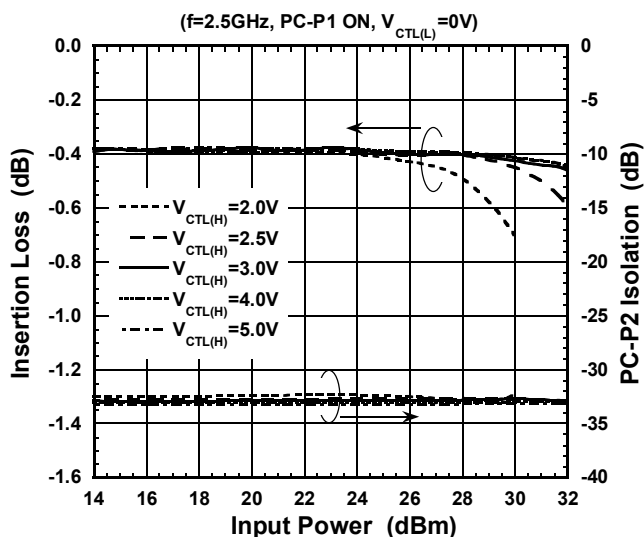
Output Power, I_{CTL} vs Input Power



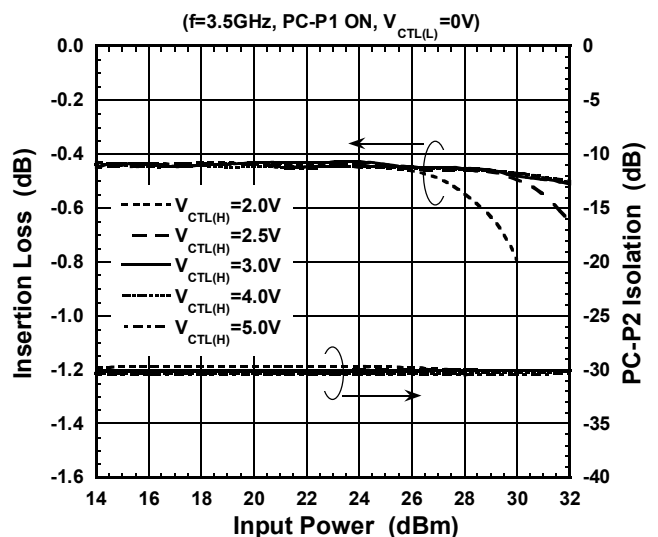
Switching Time Characteristic



Loss, ISL vs Input Power



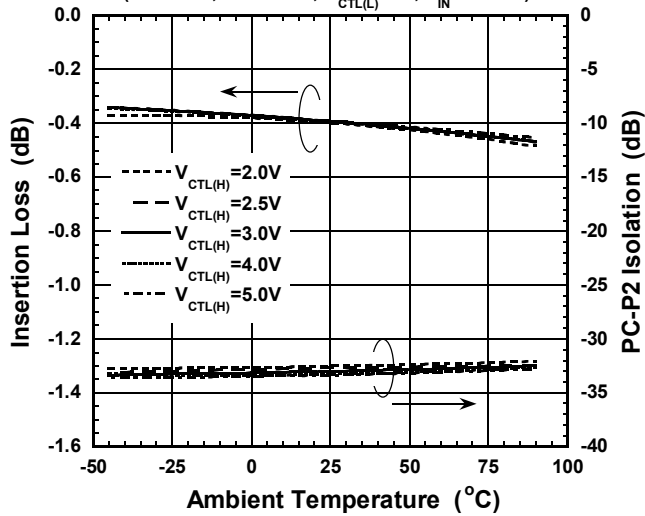
Loss, ISL vs Input Power



■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

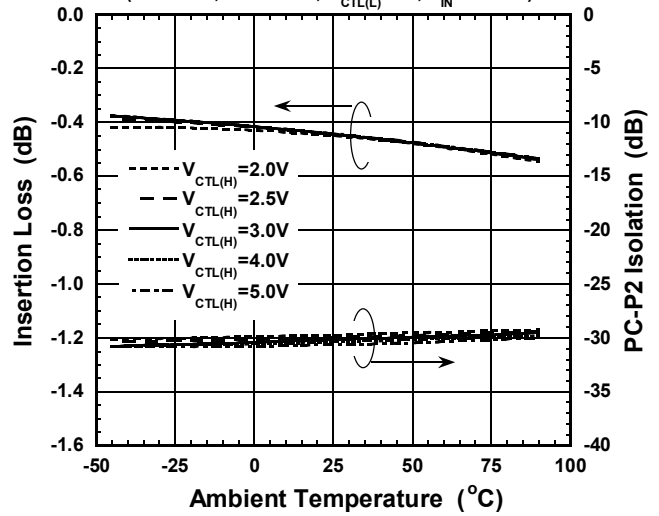
LOSS, ISL vs Temperature

(f=2.5GHz, PC-P1 ON, $V_{CTL(L)}=0V$, $P_{IN}=25dBm$)



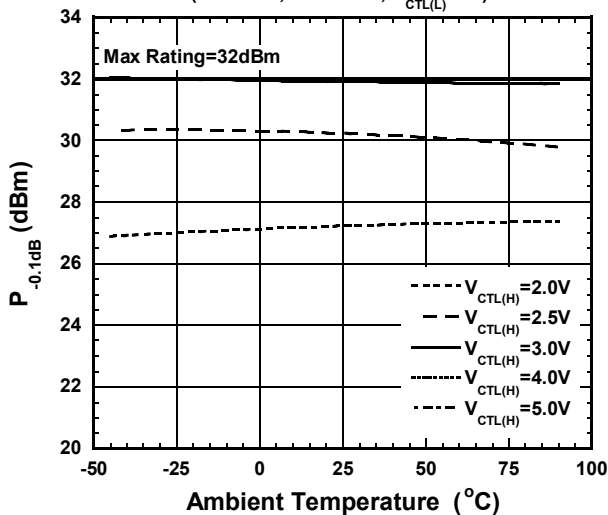
LOSS, ISL vs Temperature

(f=3.5GHz, PC-P1 ON, $V_{CTL(L)}=0V$, $P_{IN}=25dBm$)



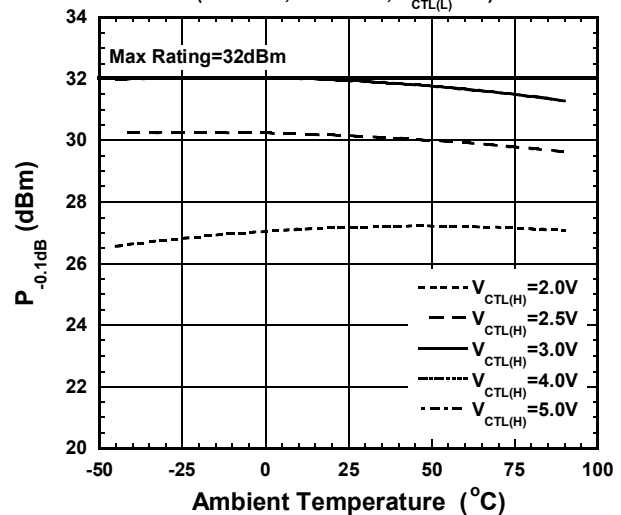
P_{-0.1dB} vs Temperature

(f=2.5GHz, PC-P1 ON, $V_{CTL(L)}=0V$)



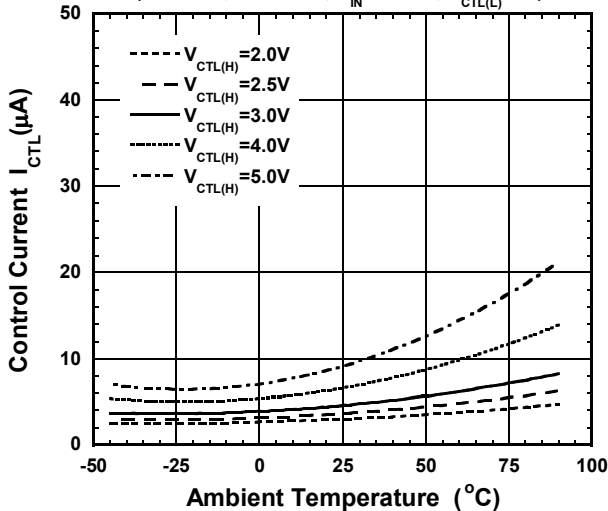
P_{-0.1dB} vs Temperature

(f=3.5GHz, PC-P1 ON, $V_{CTL(L)}=0V$)



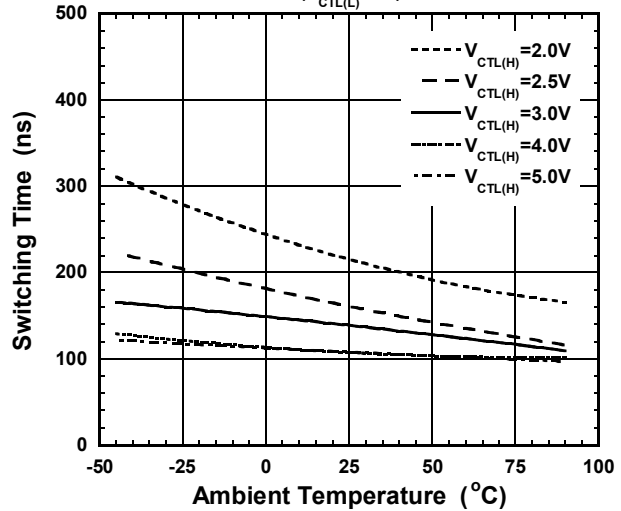
Control Current vs Temperature

(f=2.5GHz, PC-P1 ON, $P_{IN}=25dBm$, $V_{CTL(L)}=0V$)



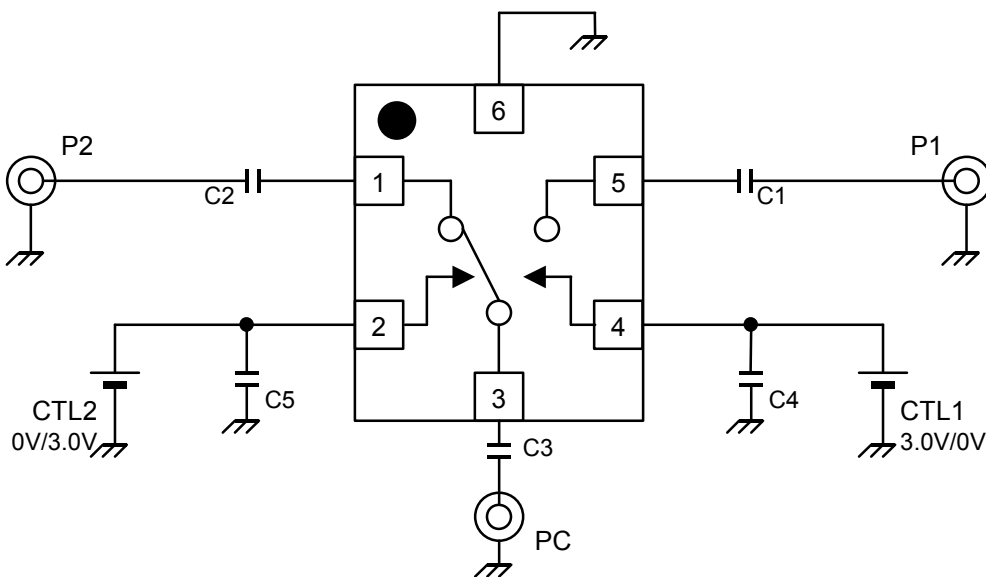
Switching Time vs Temperature

($V_{CTL(L)}=0V$)



NJG1660HA8

APPLICATION CIRCUIT

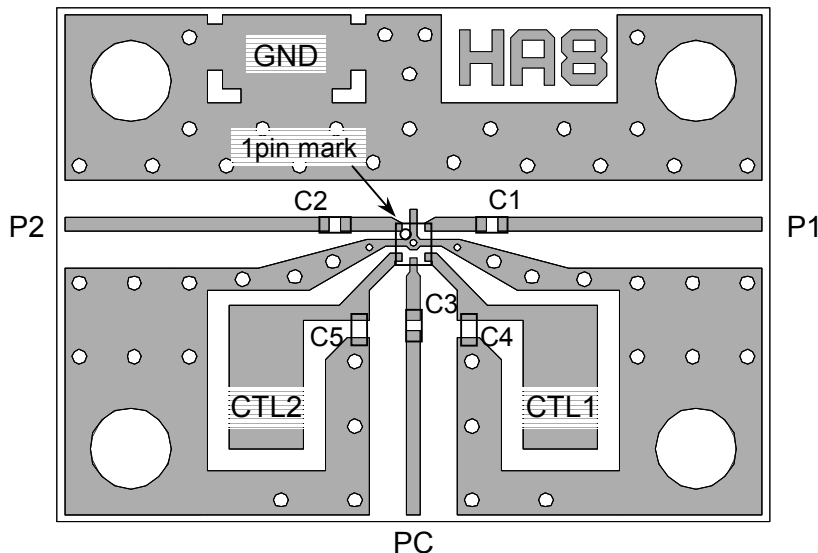


PARTS LIST

Parts ID	Value	Notes
C1~C3	27pF	Murata (GRM15)
C4, C5	10pF	

TEST PCB LAYOUT

(TOP VIEW)



PCB LOSS

Frequency (GHz)	PCB LOSS (dB)
2.5	0.38
3.5	0.47
6.0	0.73

*) Including PCB, Connector and

DC Blocking Capacitor Losses

PCB SIZE=19.4x14.0mm

PCB: FR-4, t=0.2mm

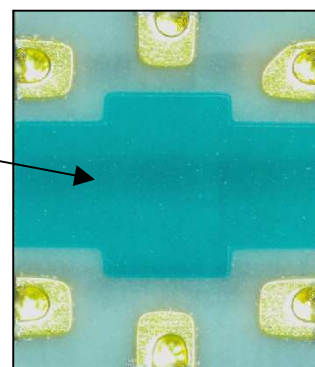
CAPACITOR: size 1005

STRIP LINE WIDTH=0.4mm

PRECAUTIONS

- [1] The DC blocking capacitors have to be placed at RF terminal of PC, P1 and P2.
- [2] For good RF performance, the ground terminals must be placed possibly close to ground plane of substrate, and through holes for GND should be placed near by the pin connection.
- [3] Bypass capacitor (C4, C5) should be placed close to terminal of CTL1 and CTL2 to reduce stripline influence of RF characteristics.

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Terminal treat	:Au
Substrate	:Glass epoxy
Molding material	:Epoxy resin
Unit	:mm
Weight	:1.1mg

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

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