# IEEE 488.2 Controller Chip Module — Drop-In Replacement for NEC µPD7210

NI NAT7210

- RoHS compliant
- Pin-compatible with NEC µPD7210
- Software-compatible with NEC µPD7210 or TI TMS9914A controller chips
- Low power consumption
- Meets all IEEE 488.2 requirements
  - Bus line monitoring
  - Preferred implementation of requesting service
  - Sends no messages when there are no listeners
- Performs all IEEE 488.1 interface functions SH1, AH1, T5 or TE5, L3 or LE3, SR1, RL1, PP1, PP2, DC1, DT1, C1, C2, C3, C4, and C5
- Reduces driver overhead Does not lose a data byte if ATN is asserted while transmitting data
- Static interrupt status bits that do not clear when read

- Programmable data transfer rate (T1 delays of 350 ns, 500 ns, 1.1 µs, and 2 µs)
- Automatic EOS and/or NL message detection
- Direct memory access (DMA)
- Automatically processes IEEE 488 commands and reads undefined commands
- Programmable compatible with bus transceivers (T1, National Semiconductor, Motorola, and Intel)
- TTL-compatible CMOS device
- Programmable clock rate up to 20 MHz
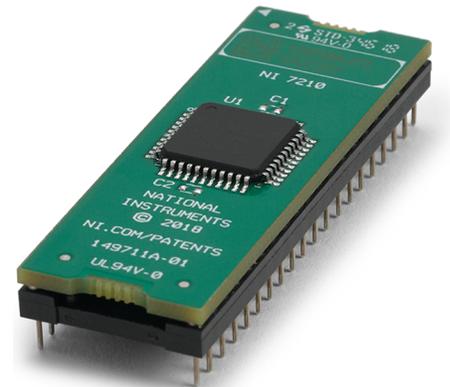
Overview

The National Instruments NAT7210 is a 40-pin DIP drop-in replacement part for the NEC µPD7210. The NAT7210 is 100 percent register and pin-compatible with the NEC µPD7210 on power up and has additional features present on the NAT4882 IEEE 488.2 controller chip. Thus, the NAT7210 can perform all the interface functions defined by the ANSI/IEEE Standard 488.1-1987 and meets the additional requirements and recommendations of ANSI/IEEE Standard 488.2-1987. The NAT7210 performs complete IEEE 488 talker, listener, and controller functions.

On power up, the NAT7210 contains the complete register set of the NEC µPD7210, but is capable of complete IEEE 488.2 controller functionality through software. An instrument developer can take advantage of IEEE 488.2 with minimal software modifications, yet retain the 40-pin hardware configuration. The default clock input is 8 MHz; however, other input values up to 20 MHz are software-selectable in the NAT7210 for increased performance. The NAT7210 can also switch to the TI 9914 register-compatible mode with a software command.

IEEE 488 instrument manufacturers looking for alternatives to existing NEC µPD7210 chip suppliers and/or planning to upgrade their designs to IEEE 488.2 without hardware changes should consider using the NAT7210. Because the NAT7210 can accept faster clock inputs, performance increases without many firmware changes.

General

The NAT7210 manages the IEEE 488 bus. You program the IEEE 488 bus by writing control words into the appropriate registers. CPU-readable status registers supply operational feedback. The NAT7210 mode determines the function of these registers. When in 7210 mode, the registers resemble the µPD7210 register set with additional registers that supply extra functionality and IEEE 488.2 compatibility. In this mode, the NAT7210 is completely pin compatible with the NEC µPD7210. When in 9914A mode, the registers resemble the TMS9914A register set with additional registers that supply extra functionality and IEEE 488.2 compatibility. Figure 2 shows the NAT7210 key components.

RoHS Compliance

The RoHS-compliant NAT7210 meets industry requirements for baking and maximum solder reflow temperature. The baking requirements are outlined in JEDEC J-STD-033, and NI recommends using the solder reflow profile as shown in IPC/JEDEC J-STD-020C with a peak temperature of 260 °C, the maximum temperature they can withstand.

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IEEE 488.2 Controller Chip Module — Drop-In Replacement for NEC µPD7210

T/R1	1		40	VCC	
T/R2	2		39	$\overline{EOI}$	
CLK	3		38	$\overline{NDAC}$	
RESET	4		37	$\overline{NRFD}$	
T/R3	5		36	$\overline{DAV}$	
DRQ	6		35	$\overline{DIO8}$	
$\overline{DACK}$	7	NAT7210	34	$\overline{DIO7}$	
$\overline{CS}$	8		33	$\overline{DIO6}$	
$\overline{RD}$	9		32	$\overline{DIO5}$	
$\overline{WR}$	10		31	$\overline{DIO4}$	
INT	11		30	$\overline{DIO3}$	
D0	12		29	$\overline{DIO2}$	
D1	13		28	$\overline{DIO1}$	
D2	14		27	$\overline{SRQ}$	
D3	15		26	$\overline{ATN}$	
D4	16		25	$\overline{REN}$	
D5	17		24	$\overline{IFC}$	
D6	18		23	RS2	
D7	19		22	RS1	
GND	20		21	RS0	
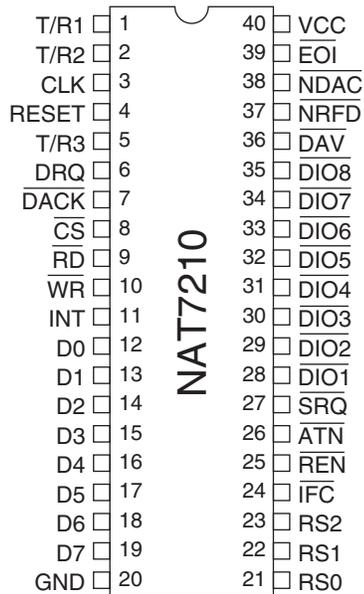
Figure 1. NAT7210 Pin Configuration
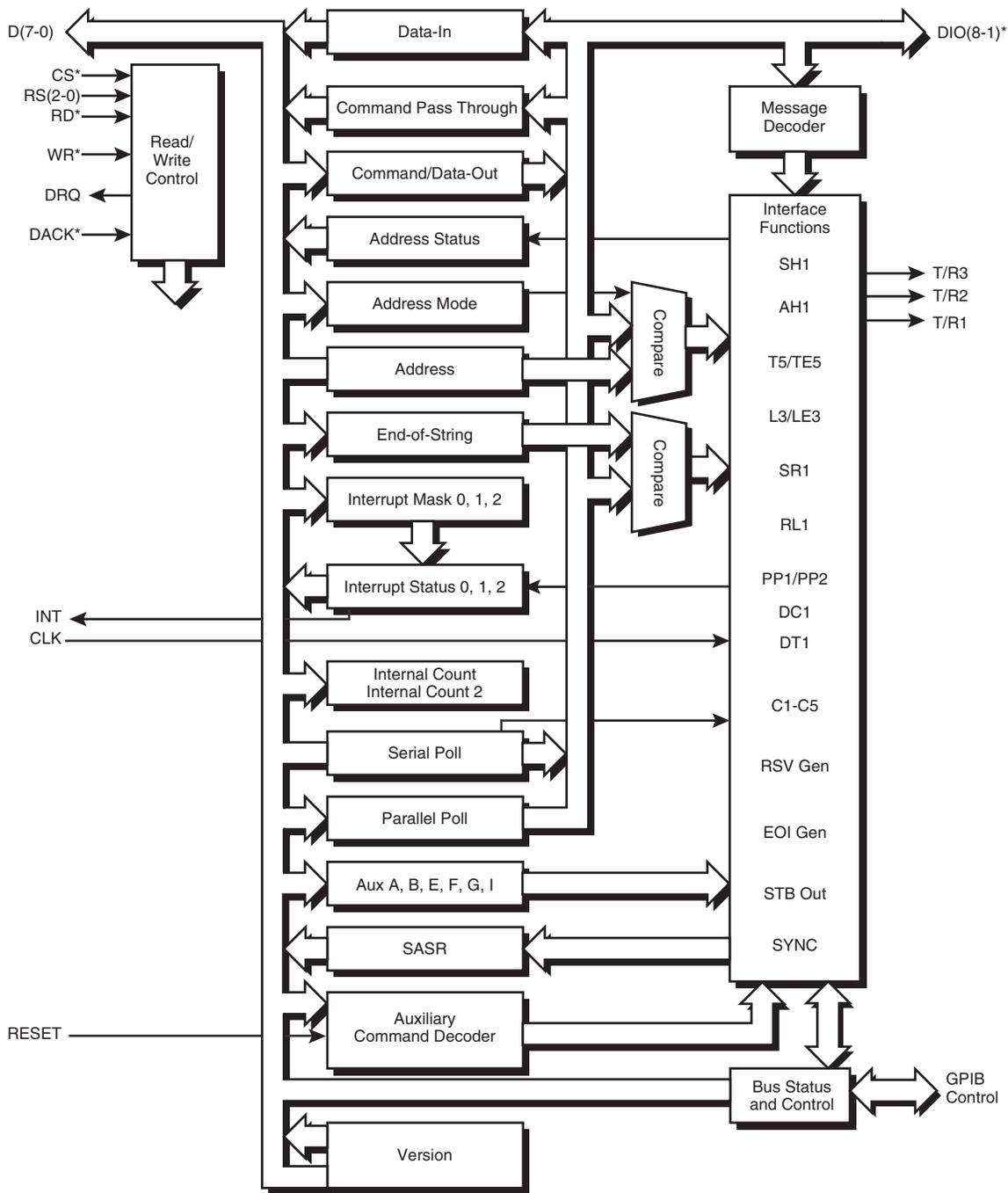
Figure 2. NAT7210 Block Diagram

Pin Descriptions

The following table describes the NAT7210 pins. For more information, refer to the *NAT7210 Reference Manual* at ni.com.

Pin Identification

Pin No.	Mnemonic	Type	Description
19, 18, 17, 16, 15, 14, 13, 12	D(7-0)	I/O	Bidirectional 3-state data bus transfers commands, data, and status between the NAT7210 and the CPU
23, 22, 21	RS(2-0)	I†	The register selects determine which register to access during a read or write operation
8	CS*	I	Chip select gives access to the register selected by a read or write operation and the register selects RS(2-0)
9	RD*	I	With the read input, you can place the contents of the register that RS(2-0) and CS* selects onto the data bus D(7-0)
10	WR*	I†	The write input latches the contents of the data bus D(7-0) into the register that RS(2-0) selects
7	DACK*	I†	The DMA acknowledge signal selects the DIR or CDOR for the current read or write cycle
6	DRQ	O	The DMA Request output asserts to request a DMA acknowledge cycle
3	CLK	I	The CLK input can be up to 20 MHz
4	RESET	I	Asserting the reset input places the NAT7210 in an initial, idle state
11	INT	O†	The Interrupt output asserts when one of the unmask interrupt conditions is true
24	IFC*	I/O†	Bidirectional control line initializes the IEEE 488 interface functions
25	REN*	I/O†	Bidirectional control line selects either remote or local control of devices
26	ATN*	I/O†	Bidirectional control line indicates whether data on the DIO lines is an interface or device-dependent message
27	SRQ*	I/O†	Bidirectional control line requests service from the Controller
35, 34, 33, 32, 31, 30, 29, 28	DIO(8-1)*	I/O	8-bit bidirectional IEEE 488 data bus
36	DAV*	I/O†	Handshake line indicates that the data on the DIO(8-1)* lines is valid
37	NRFD*	I/O†	Handshake line indicates that the device is ready for data
38	NDAC*	I/O†	Handshake line indicates the completion of a message reception
39	EOI*	I/O†	Bidirectional control line indicates the last byte of a data message or executes a parallel poll
1	T/R1	O	Talk Enable controls the direction of the IEEE 488 data transceiver
5	T/R3	O	These pins are the input/output control for the IEEE 488 transceivers
2	T/R2		
40	VCC	–	Power pin +5 V (±5%)
20	GND	–	Ground pin – 0 V

† The pin contains an internal pull-up resistor of 25 to 100 kΩ.
* Active low.

Table 1. NAT7210 APD Pin Configuration
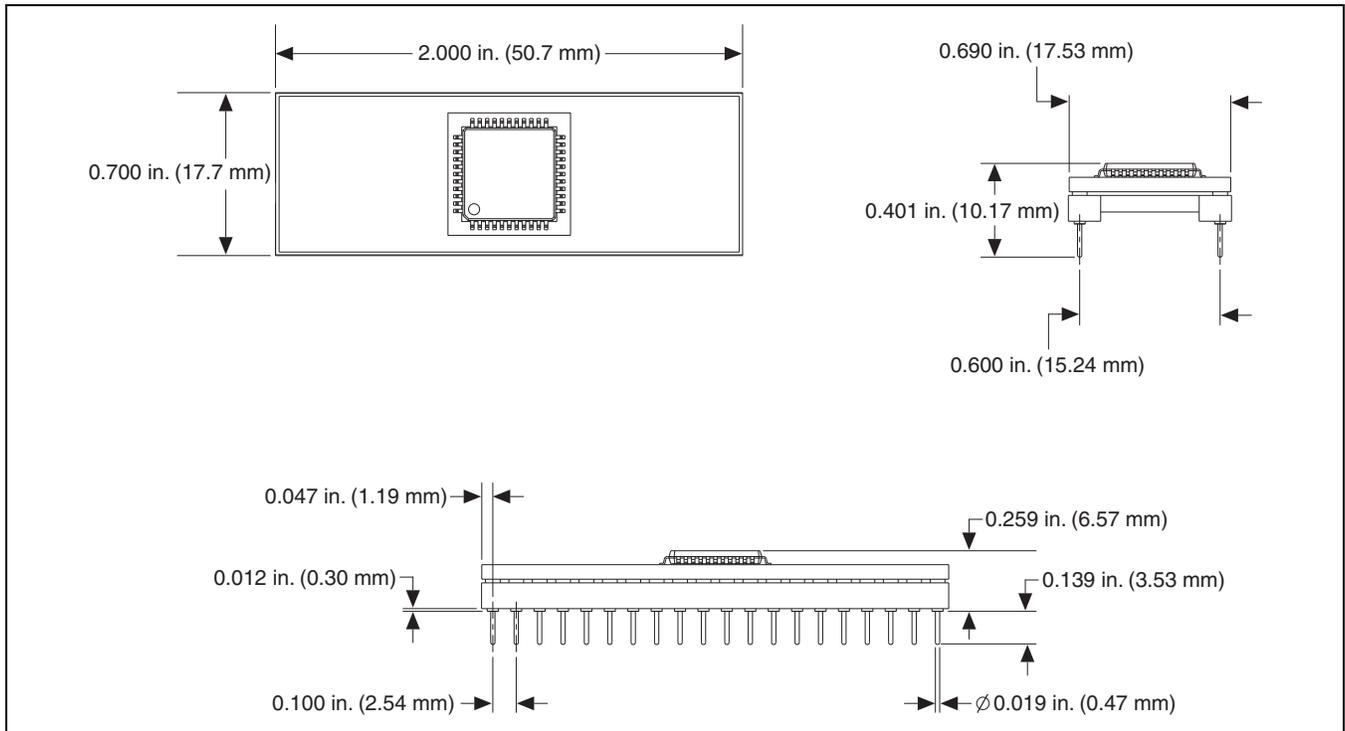
Mechanical Data

Figure 3. Mechanical Data 40-Pin Plastic DIP Package Compatible Module

7210 Mode Registers

In 7210 mode, the NAT7210 registers include all the NEC µPD7210 registers plus two types of additional registers – extra auxiliary registers and paged-in registers. You write the extra auxiliary registers the same as standard µPD7210 auxiliary registers. Upon issuing an auxiliary page-in command, the paged-in registers appear at the same offsets as existing µPD7210 registers. At the end of the next CPU access, the chip pages out the paged-in registers. The following table lists all the registers in the 7210 mode register set.

For programming information, refer to the *NAT7210 Reference Manual* at ni.com.

7210 Register Set

Register	PAGE-IN	A(2-0)	WR*	RD*	CS*	DACK*
Data-in	U	0 0 0	1	0	0	1
Data-in	X	X X X	1	0	X	0
Command/data-out	U	0 0 0	0	1	0	1
Command/data-out	X	X X X	0	1	X	0
Interrupt status[1]	U	0 0 1	1	0	0	1
Interrupt mask[1]	U	0 0 1	0	1	0	1
Interrupt status[2]	U	0 1 0	1	0	0	1
Interrupt mask[2]	U	0 1 0	0	1	0	1
Serial Poll status	N	0 1 1	1	0	0	1
Serial Poll mode	N	0 1 1	0	1	0	1
Version	P	0 1 1	1	0	0	1
Internal counter[2]	P	0 1 1	0	1	0	1
Address status	U	1 0 0	1	0	0	1
Address mode	U	1 0 0	0	1	0	1
Command pass through	N	1 0 1	1	0	0	1
Auxiliary mode	U	1 0 1	0	1	0	1
Source/acceptor status[†]	P	1 0 1	1	0	0	1
Address 0	N	1 1 0	1	0	0	1
Address	N	1 1 0	0	1	0	1
Interrupt status 0[†]	P	1 1 0	1	0	0	1
Interrupt mask 0[†]	P	1 1 0	0	1	0	1
Address[†]	N	1 1 1	1	0	0	1
End-of-string	N	1 1 1	0	1	0	1
Bus status[†]	P	1 1 1	1	0	0	1
Bus control[†]	P	1 1 1	0	1	0	1

Notes for the Page-In column
U = The page-in auxiliary command does not affect the register.
N = The register offset is always valid except for immediately after a page-in auxiliary command.
P = The register is valid only immediately after a page-in auxiliary command.
The '†' symbol denotes features (such as registers and auxiliary commands) that are not available in the µPD7210.

9914 Mode Registers

In 9914 mode, the NAT7210 registers consist of all the TI TMS9914A registers and two types of additional registers – newly defined registers and paged-in registers. The NAT7210 maps the newly defined registers into the unused portion of the 9914 address space. Each paged-in register appears at offset two immediately after you issue an auxiliary page-in command and remains there until you either page another register into the same space or issue a reset. The following table lists all the registers in the 9914 register set. Refer to the *NAT7210 Reference Manual* at ni.com for more information.

9914 Register Set

Register	Page In	RS(2-0)	WR*	RD*	CS*	DACK*
Interrupt status 0	U	0 0 0	1	0	0	1
Interrupt mask 0	U	0 0 0	0	1	0	1
Interrupt status 1	U	0 0 1	1	0	0	1
Interrupt mask 1	U	0 0 1	0	1	0	1
Address status	U	0 1 0	1	0	0	1
Interrupt mask 2[†]	P	0 1 0	0	1	0	1
End-of-string[†]	P	0 1 0	0	1	0	1
Bus control[†]	P	0 1 0	0	1	0	1
Accessory[†]	P	0 1 0	0	1	0	1
Bus status	U	0 1 1	1	0	0	1
Auxiliary command	U	0 1 1	0	1	0	1
Interrupt status 2[†]	P	1 0 0	1	0	0	1
Address	U	1 0 0	0	1	0	1
Serial poll status[†]	P	1 0 1	1	0	0	1
Serial poll mode	U	1 0 1	0	1	0	1
Command pass thru	U	1 1 0	1	0	0	1
Parallel poll	U	1 1 0	0	1	0	1
Data-in	U	1 1 1	1	0	0	1
Data-in	U	X X X	1	0	X	0
Command/data-out	U	1 1 1	0	1	0	1
Command/data-out	U	X X X	0	1	X	0

Notes for the Page-In column
U = Page-in auxiliary commands do not affect the register offset.
P = The register offset is valid only after a page-in auxiliary command.
The '†' symbol denotes features (such as registers and auxiliary commands) that are not available in the TMS9914A.

DC Characteristics

TA$_0$ to 70 °C; V$_{CC}$ = 5 V ±5%

Parameter	Symbol	Limits		Unit	Test Condition
		Min	Max		
Voltage input low	VIL	-0.5	+0.8	V	
Voltage input high	VIH	+2.0	VCC	V	
Voltage output low	VOL	0	0.4	V	
Voltage output high	VOH	+2.4	VCC	V	
Input/output leakage current		-10	+10	µA	without internal pull up
Input/output leakage current		-200	+200	µA	with internal pull up
Supply current			45	mA	
Output current low All pins except T/R1	IOL	2		mA	VOL = 0.4 V
T/R1	IOL	4		mA	VOL = 0.4 V
Input current low/high	IIL		-0.5	mA	
Output current high	IOH	-1		mA	VOH = VCC - 0.5 V
Supply voltage	VCC	4.75	5.25	V	

Capacitance

TA$_0$ to 70 °C; V$_{CC}$ = 5 V ±5%

Parameter	Symbol	Limits		Unit	Test Condition
		Min	Max		
Input capacitance	Cin		10	pF	
Output capacitance	Cout		10	pF	
I/O capacitance	CI/O		10	pF	

Absolute Maximum Ratings

Property	Range
Supply voltage, VCC	-0.5 to +6.0 V
Input voltage, VI	-0.5 to VCC +0.5
Operating temperature, TOPR	0 to +70 °C
Storage temperature, TSTG	-40 to +125 °C

Comment – exposing the device to stresses above those listed could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC Characteristics

TA$_0$ to 70 °C; V$_{CC}$ = 5 V ±5%

Parameter	Symbol	Limits		Unit	Test Condition
		Min	Max		
Address hold from $\overline{RD}\uparrow$, $\overline{WR}\uparrow$	t_{AH}	0		ns	
Address setup to $\overline{RD}\downarrow$, $\overline{WR}\downarrow$	t_{AS}	0		ns	
Data float from $\overline{RD}\uparrow$	t_{DF}		25	ns	
Data delay from $\overline{RD}\downarrow$	t_{DR}		80	ns	DACK = 0
DRQ unassertion	t_{DU}		25	ns	
Data delay from $\overline{RD}\downarrow$	t_{RD}	85		ns	CS = 0
RD recovery width	t_{RR}	120		ns	
RD pulse width	t_{RW}	85		ns	
Data setup to $\overline{WR}\uparrow$	t_{WS}	60		ns	
Data hold from $\overline{WR}\uparrow$	t_{WH}	0		ns	

Timing Waveforms
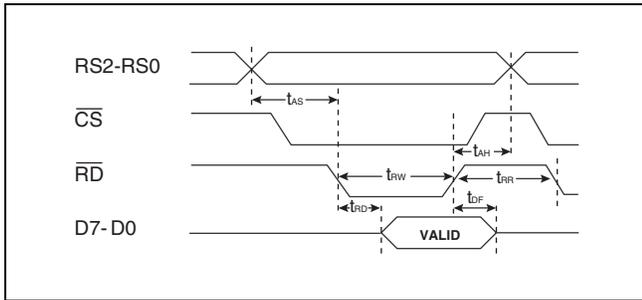

Figure 4. CPU Read
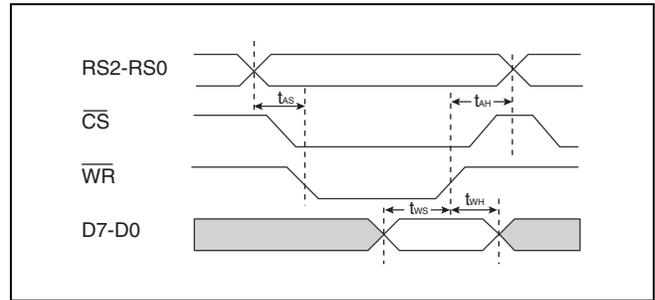
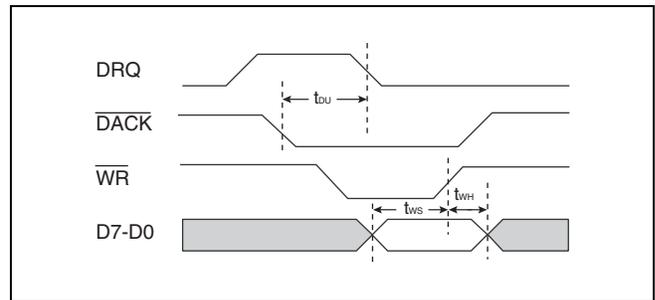**Figure 6.** CPU Write
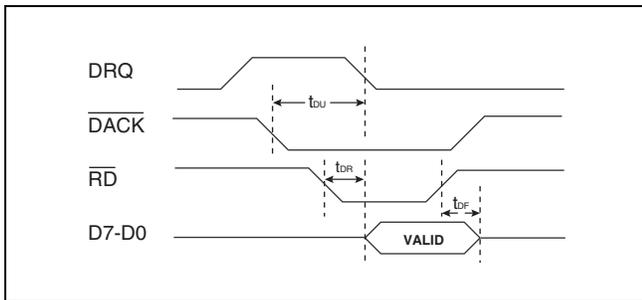
Figure 5. DMA Read

Figure 7. DMA Write

Source Handshake

Parameter	Symbol	Limits		Test Condition
		Min	Max	
$\overline{NDAC}$↑ to $\overline{DAV}$↑	t_{ND}		40	
$\overline{NDAC}$↑ to INT↑ or DRQ↑	t_{NI}		40	INT (DO IE Bit = 1) DRQ (DMAO Bit = 1)
$\overline{WR}$↑ to $\overline{DAV}$↓	t_{WD}	2,000	2,125	2 μs T1 (8 MHz, 50% duty)
$\overline{WR}$↑ to $\overline{DAV}$↓	t_{WD}	1,125	1,250	1.1 μs T1 (8 MHz, 50% duty)
$\overline{WR}$↑ to $\overline{DAV}$↓	t_{WD}	500	625	500 ns T1 (8 MHz, 50% duty)
$\overline{WR}$↑ to $\overline{DAV}$↓	t_{WD}	375	500	350 ns T1 (8 MHz, 50% duty)
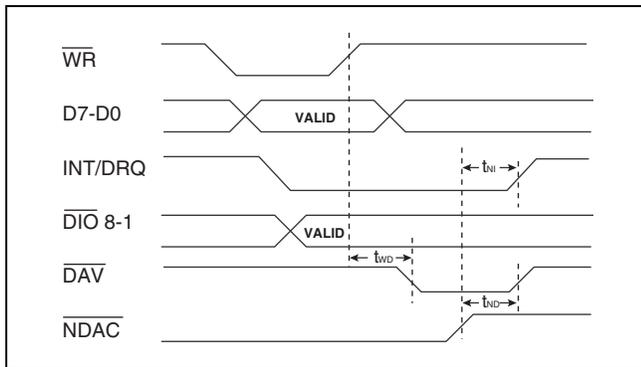
Figure 8. Source Handshake

Acceptor Handshake

Parameter	Symbol	Limits		Test Condition
		Min	Max	
$\overline{DAV}$↓ to $\overline{NDAC}$↑	t_{DD}		225	8 MHz 50% duty
$\overline{DAV}$↑ to $\overline{NDAC}$↓	t_{DF}		20	
$\overline{DAV}$↓ to INT↑ or DRQ↑	t_{NI}		116	INT (DIIE Bit = 1), DRQ (DMAI Bit = 1) 8 MHz, 50% duty
$\overline{DAV}$↓ to $\overline{NRFD}$↓	t_{DR}		25	
$\overline{RD}$↑ to $\overline{NRFD}$↑	t_{NR}		30	Read of DIR, not in Holdoff state
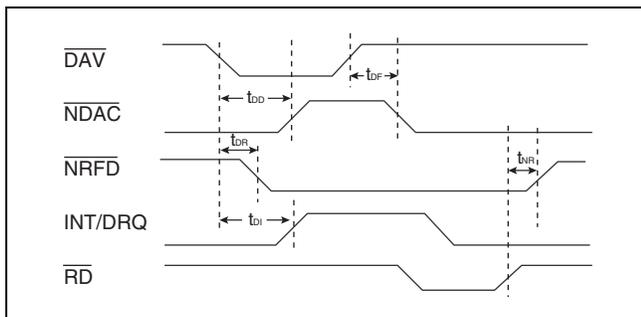
Figure 9. Accepter Handshake

Response to ATN

Parameter	Symbol	Limits		Test Condition
		Min	Max	
$\overline{ATN}$↑ to $\overline{NRFD}$↓	t_{AF}		35	Acceptor handshake Holdoff
$\overline{ATN}$↓ to $\overline{NDAC}$↓	t_{AN}		35	AIDS → ANRS
$\overline{ATN}$↓ to TE↓	t_{AT}		30	TACS → TADS
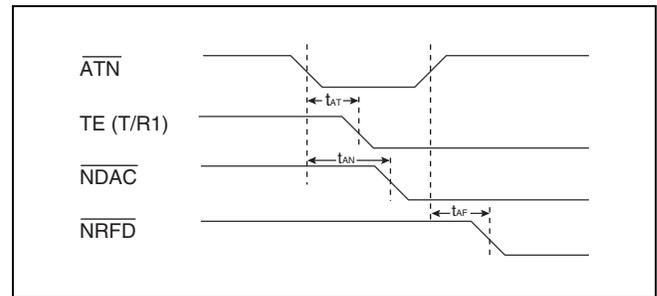
Figure 10. Response to WATN

Parallel Poll

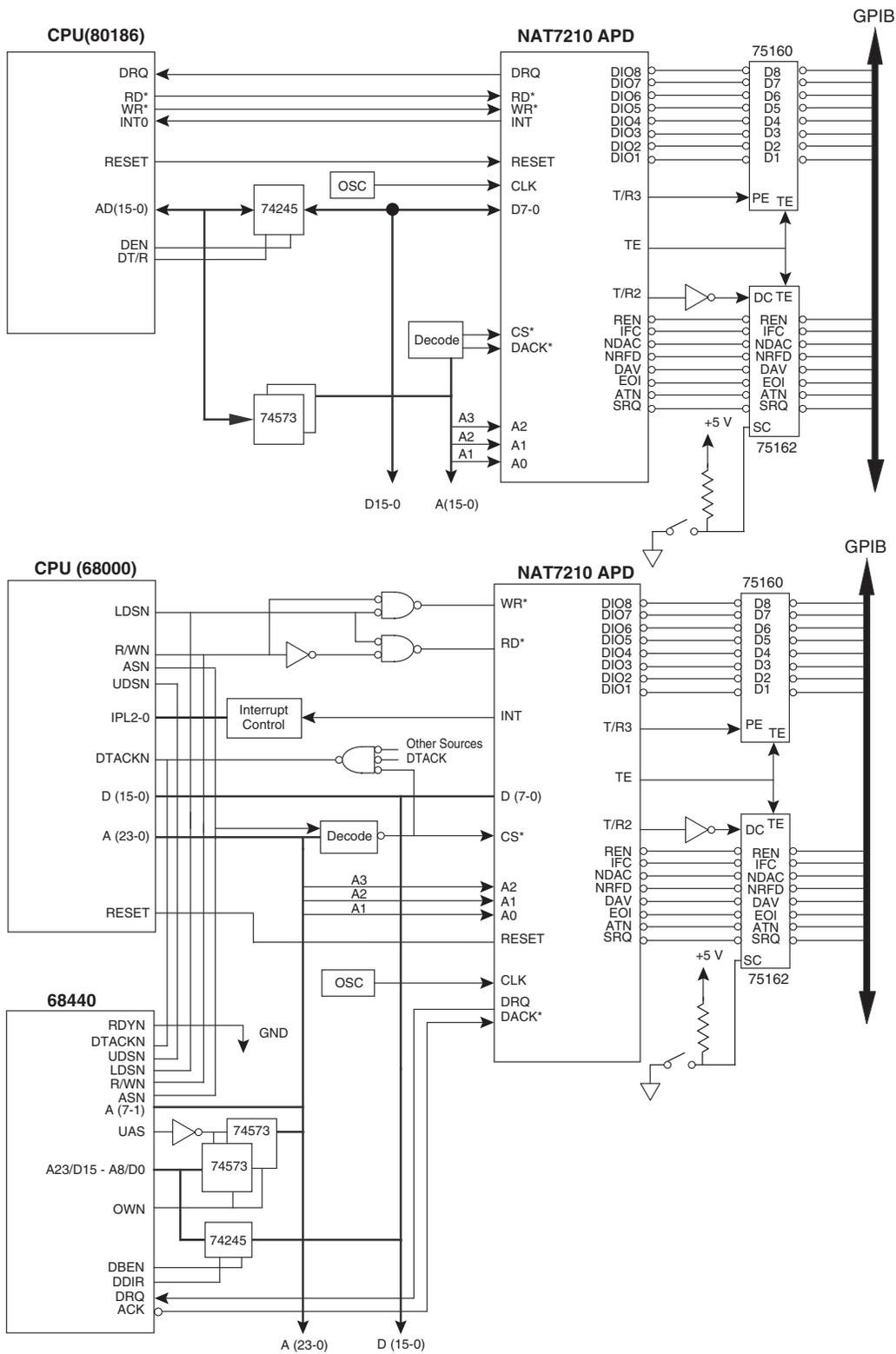| Parameter	Symbol	Limits		Test Condition
		Min	Max	
$\overline{EOI}$↓ to $\overline{DIO}$ valid	t_{ED}		90	PPSS › PPAS
$\overline{EOI}$↓ to TE↑	t_{ET}		25	PPSS › PPAS
$\overline{EOI}$↑ to TE↓	t_{TE}		25	PPAS › PPSS
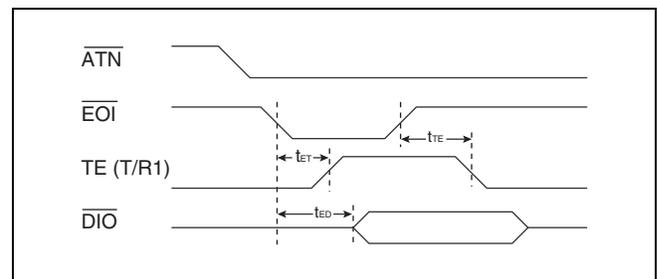
Figure 11. Parallel Poll

Figure 12. Typical CPU Systems wih NAT7210

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