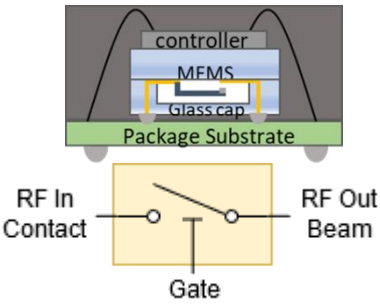
Preliminary Datasheet
MM3100 – 6 Channel SPST RF Micro Switch

Product Overview

Description

The MM3100 device is a high power, normally open (NO), six channel Single Pole Single Throw (SPST) micro-mechanical switch for RF and microwave switch applications. The MM3100 is based on Menlo's Ideal Switch™ technology and is capable of 25 W power transfer. Each channel provides ultra-low on-state insertion loss and high off-state isolation from DC to over 3.0 GHz with greater than 3 billion switching cycles. Each channel can be individually controlled by a serial-to-parallel interface that drives the gate lines of the switches. The flexibility of six SPST channels enable implementation of different signal topologies such as dual SP3T, triple SP2T or 2 x 3 matrix. Only an external logic supply and gate bias source are required for operation of the device.

Features



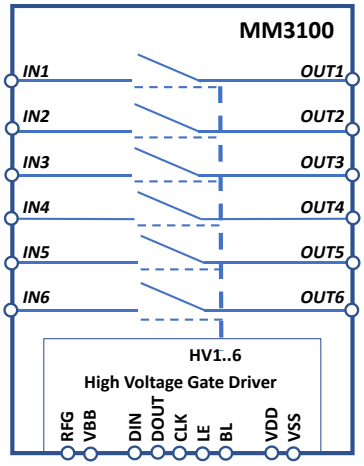
- DC to 3.0 GHz Frequency Range
- 25 W (CW), 200 W (Pulsed) Max Power Handling
- Low On-State Insertion Loss, typical 0.3 dB @ 3.0 GHz
- Low On-State Resistance < 1 Ω typical
- 25 dB Isolation @ 3 GHz
- Maximum Voltage (AC_{Peak} or DC): +/-150 Volts on RF Input
- Switching Time < 10 us
- High Reliability > 3 Billion Switching Operations
- Integrated driver eliminates requirement for an external gate driver
- 6 mm x 6 mm BGA Package

Applications

- High-Power Tunable Resonators and Filters
- Broadband Power Amplifier Impedance Matching
- Electronically Steerable Antennas and Phase Shifters
- Automated Test and Measurement Systems

Markets

- Defense and Aerospace
- Scientific and Medical
- Wireless Infrastructure



Electrical Characteristics

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM3100 should be restricted to the limits indicated in the recommended operating conditions listed in Tables 2 to 5.

Electrostatic Discharge (ESD) Safeguards

The MM3100 is a Class 0 ESD device. When handling the MM3100, observe precautions as with any other ESD sensitive device. Do not exceed the voltage ratings specified in Table 1 below.

Power Sequencing

The following power sequence is recommended:

- Power-Up: Apply VDD, set all inputs to known state, apply VBB
- Power-Down: Remove VBB, remove all inputs, remove VDD

The high voltage supply (VBB) may be applied and removed as required when VDD is present. VBB voltage should not drop below VDD or float during operation.

Table 1 Absolute Maximum Ratings[1]

Parameter	Minimum	Maximum	Unit
Driver Voltage Supply (VDD)		7.5	V_{DC}
High Voltage Gate Supply (VBB)		90	V_{DC}
Driver Logic Input Levels	-0.3	V_{DD} + 0.3	V
CW Input Power / Channel		25	W
DC Voltage VBB to OUTx pin (V_{VBB_OUT})	-100	100	V
Open State Voltage INx to OUTx[2,3]	-150	150	V

[1] All parameters must be within recommended operating conditions. Maximum DC and RF power can only be applied during the on-state condition (cold-switched condition). CW Input Power Rating in 50 Ω environment, VSWR = 1.
[2] This also applies to ESD events. This is a Class 0 device.
[3] The voltage difference between RF Output (Beam) pin and Supply Voltage Return (VSS) pin must be within ±2.5V. Ideally the VSS pin is tied to a node with the same potential as signal ground. This ties the GATE to ground potential in the off state.

Open State Voltage OUT1-OUT6, IN1-IN6 to GND	-150	150	V
Hot Switching Voltage[4]	-0.5	0.5	V
DC Carry Current / Channel		1000	mA
Total Carry Current per Device		3000	mA
Operating Temperature Range	-40	+85	ºC
Storage Temperature Range[5]	-65	+150	ºC
ESD Rating HBM Driver Pins[6]		TBD	V
ESD Rating HBM RF I/O Pins[7] [8]		150	V
Mechanical Shock[9]		500	G
Vibration[10]		500	Hz

[4] See section Hot Switch Restrictions for more information.
[5] See section Storage and Shelf Life for more information on shelf and floor life.
[6] Driver pins include: CLK, LE, DIN, DOUT, BL, VBB, VDD.
[7] RF I/O pins include: IN1 to IN6, OUT1 to OUT6.
[8] RF I/O pins must not be allowed to electrically float during switch operation. See section *Floating Node Restrictions* for details on avoiding floating nodes.
[9] See JESD22-B104 for mechanical shock test methodology at 1.0 ms, half-sine, 5 shocks/axis, 6 axis.
[10] See JESD22-B103 for vibration test methodology at 3.1 G and 30min/cycle, 1 cycle/axis, 3 axis.

Recommended Operating Conditions

All specifications valid over full VBB range and operating temperature range unless otherwise noted.

Table 2 RF Characteristics

Parameter	Minimum	Typical	Maximum	Unit
Operating Frequency Range	DC		3.0	GHz
CW Power / Channel[11]			25	W
Peak Power / Channel @ 10% Duty Cycle[12]			200	W
Insertion Loss @ 3.0 GHz		0.3		dB
Input / Output Return Loss @ 3.0 GHz		15		dB
Input to Output Isolation @ 3.0 GHz		18		dB
Adjacent Channel Isolation @ 3.0 GHz[13] Both Channels Closed One Channel Open		 25 TBD		dB
Third-Order Output Intercept (IP3)		85		dBm
Second Harmonic (H2)[14]		TBD		dBc
Third Harmonic (H3)[15]		TBD		dBc

Table 3 DC and AC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
DC Carry Current / Channel			1000	mA
On / Closed State Output to VSS Voltage	TBD		TBD	V_{DC}
On / Off Switching and Settling Time[16] Turn on time Turn off time		 8.5 2.5	 16 6	µs

[11] Maximum allowable Continuous Wave Power below 2.0 MHz is 1.0 W.
[12] Duty Cycle based on 10 us period.
[13] See section Adjacent Channel Isolation for more information regarding isolation measurements.
[14] Measured at 1.0 GHz and 2.0 GHz fundamental frequency and 35 dBm input power.
[15] Measured at 1.0 GHz and 2.0 GHz fundamental frequency and 35 dBm input power.
[16] Includes any actuator bounce, settling time to within 0.05dB of final value, and measured with 20 V/us slew rate GATE pin voltage.

Full Cycle Frequency			10	kHz
On / Off Switch Operations (Cold Switched)	3 x 10^9	TBD		Cycle
Off-State Input–Output Leakage @ 150 V		25	TBD	pA
On-State Resistance		1.0	3.0	Ω
Off-State Capacitance (C_{Off}) [17]		90		fF
High Voltage Gate Bias VBB (V_{BB})	78	79	80	V_{DC}
High Voltage Gate Bias VBB Current (I_{BB})		0.05	0.1	mA

Table 4 Driver DC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
Driver Logic Supply VDD Voltage (V_{DD})	4.5	5.0	5.5	V_{DC}
Driver Logic Supply VDD Current in standby (I_{DD})		10	50	uA
Driver Input (DIN) @ VDD=5.0V				
High-Level Logic Voltage V_{IH}	3.5	5.0	5.3	V
Low-Logic Input Voltage V_{IL}	-0.3		0.8	V
High-Logic Input Current I_{IH}			1	uA
Low-Logic Input Current I_{IL}			TBD	uA
Driver Output (DOUT) VDD=4.5V				
High-Level Logic Output V_{OH} [18]	4		-	V
Low-Level Logic Output V_{OL} [19]	-		1.0	

[17] Capacitance between input and output pins.
[18] V_{OH} measured at ID_{OUT} = -0.1 mA.
[19] V_{OL} measured at ID_{OUT} = -0.1 mA.

Table 5 Driver Interface AC Electrical Specifications

Parameter	Minimum	Typical	Maximum	Unit
Clock Frequency f_{CLK}	0		5	MHz
Clock Width High and Low t_{WL},t_{WH}	100			ns
Data Setup Time before Clock Rises t_{SU}	50			ns
Data Hold Time after Clock Rises t_H	50			ns
Latch Enable Pulse Width t_{WLE}	100			ns
Latch Enable Delay Time after Rising Edge of Clock t_{DLE}	50			ns
All Logic Inputs t_r, t_f			5	ns

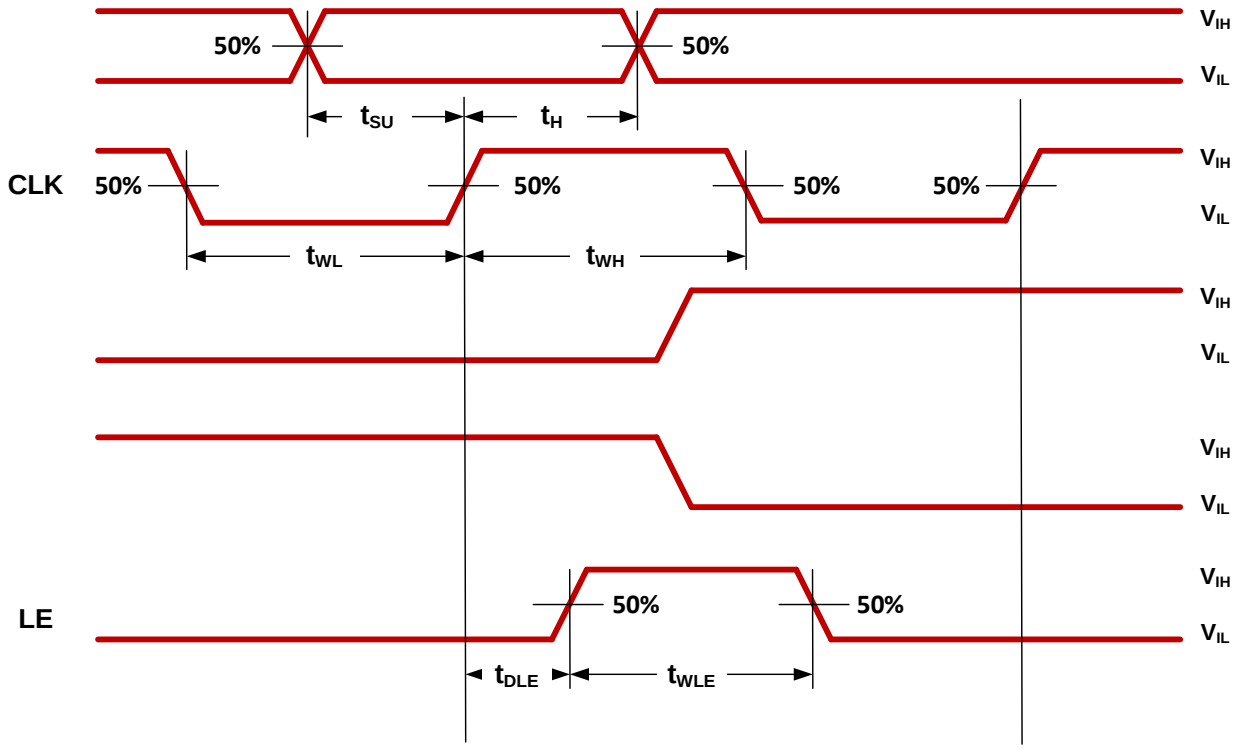


Figure 1: Driver Interface Timing Diagram

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Hot Switch Restrictions

The MM3100 is not intended for hot switching applications and care should be taken to insure that switching occurs at less than 0.5 V. Further, the voltage at the switch terminals must be within +/-0.5 V relative to RF ground.

Floating Node Restrictions

RF I/O pins must not be allowed to electrically float during switch operation and therefore require some form of DC path to ground to prevent charge accumulation. DC paths can be an inductor or high value resistance which serves as a discharge path. Floating node examples are:

- Unconnected RF pins, resistively terminate or tie to ground.
- Series capacitance coupling which floats RF pin, shunt with DC path to ground.

See Menlo Micro application note ***Avoiding Floating Nodes*** for detailed explanation of the hazard conditions to avoid and recommended solutions.

Functional Block Diagram

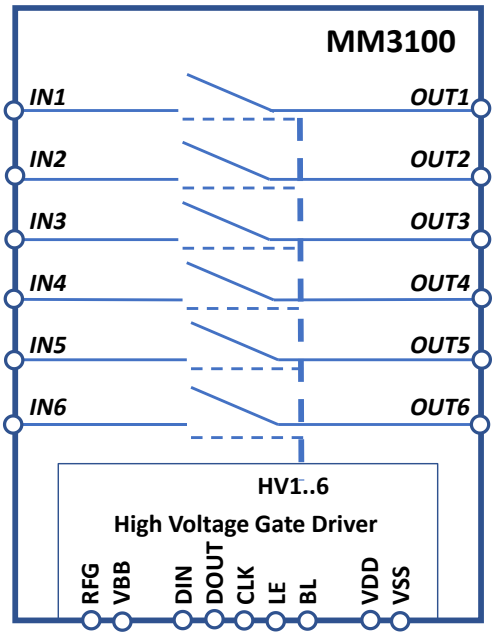


Figure 2: Functional Block Diagram

49-Lead BGA Package Pinout

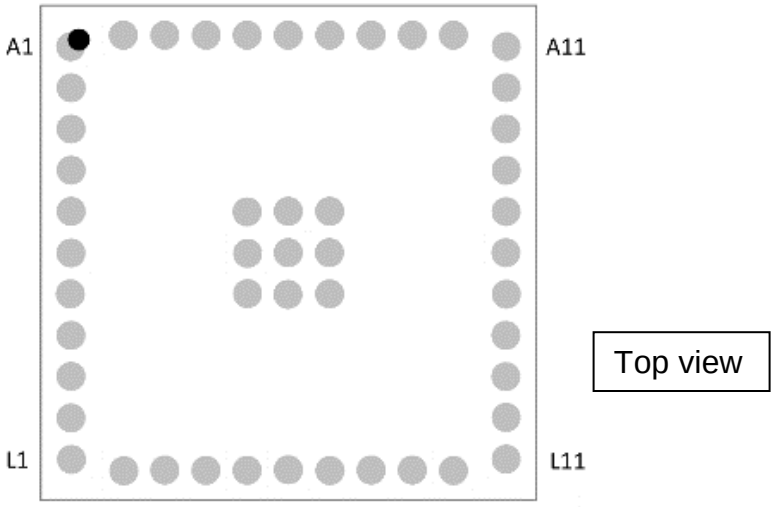


Figure 3: Top View Pin Layout

See **Table 6 Detailed Pin Description** below for detailed pin description.

Table 6 Detailed Pin Description

Pin #	Name	Description	Pin #	Name	Description
A1, C1, J1, L1, L2, L4, L6, L8, L10, L11, J11, C11, A10, A11, A6, A8, A2, A4, E5, E6, E7, F5, F6, F7, G5, G6, G7	RFG	RF Ground Reference, internal shield	L9	IN5	RF Input (Contact 5)
B1	OUT1	RF Output (Beam 1)	K11	IN6	RF Input (Contact 6)
D1	BL	All Channels Off	H11	CLK	Driver Clock Input
E1	DIN	Driver Serial Data Input	G11	VSS	Supply Voltage Return
F1, D11	N/C	Do Not Connect	F11	VDD	Driver Logic Supply
G1	VBB	Gate Bias High Voltage Supply	E11	LE	Driver Latch Input
H1	DOUT	Driver Serial Data Output	B11	OUT6	RF Output (Beam 6)
K1	IN1	RF Input (Contact 1)	A9	OUT5	RF Output (Beam 5)
L3	IN2	RF Input (Contact 2)	A7	OUT4	RF Output (Beam 4)
L5	IN3	RF Input (Contact 3)	A5	OUT3	RF Output (Beam 3)
L7	IN4	RF Input (Contact 4)	A3	OUT2	RF Output (Beam 2)

RF Performance

Typical device performance is measured on MM3100-EVK evaluation board.

Adjacent Channel Isolation

Adjacent channel (Ch) isolation is defined for the MM3100 in two ways:

1. Both channels closed: measured between Ch 3 Output and Ch 4 input. This particular combination is the worst case for channel to channel isolation.
2. Second channel open: measured between Ch 3 Output and Ch 4 input,with Ch 3 Closed and Ch 4 open.

Measurements are done at 3.0 GHz with all ports terminated with 50 Ohm during measurement as shown in Figure 4 below. Increasing channel physical separation increases isolation for the two cases as follows:

1. Both channels closed:
   - Second adjacent channel performance is typically 8 dB better than adjacent channel performance (example: Ch 2 – Ch 4).
   - Third adjacent channel performance is typically 15 dB better than adjacent channel performance (example: Ch 1 – Ch 4).
2. Second channel open:
   - Second adjacent channel performance is typically 13 dB better than adjacent channel performance (example: Ch 2 – Ch 4).
   - Third adjacent channel performance is typically 17 dB better than adjacent channel performance (example: Ch 1 – Ch 4).

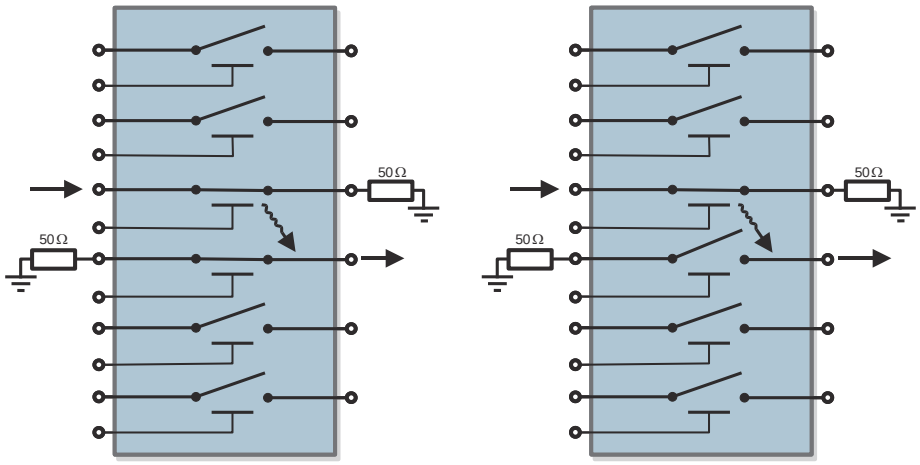
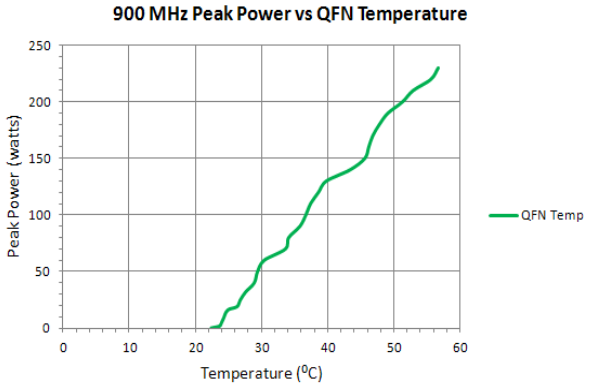
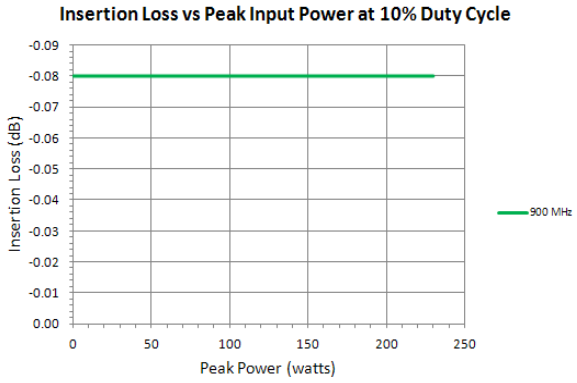


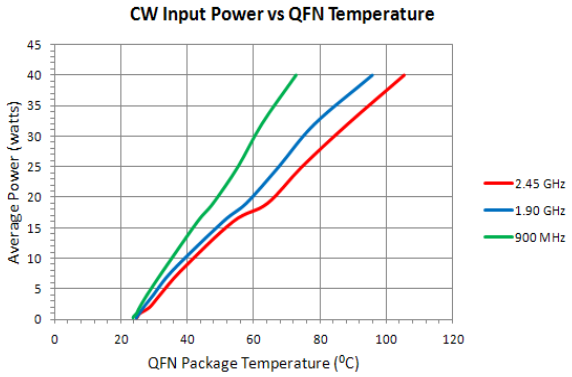
Figure 4: Adjacent Channel Isolation Measurement

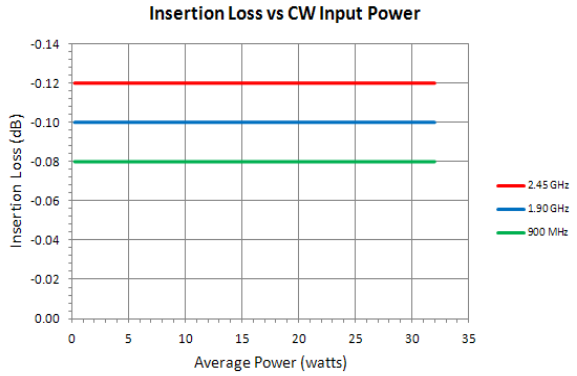




1. Peak Input Power at +25°C

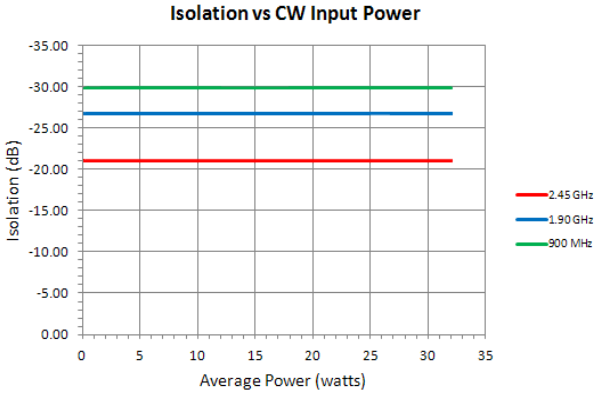
2. Peak Power Insertion Loss at +25°C

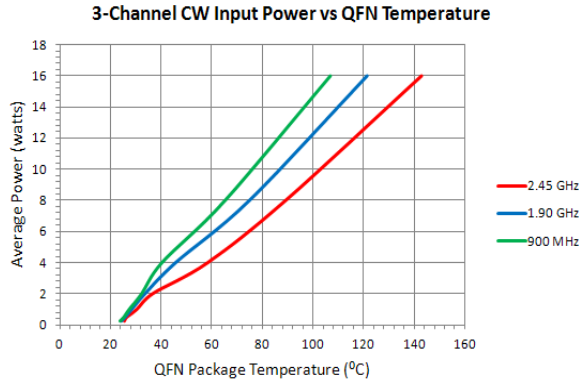




3. CW Input Power at +25°C

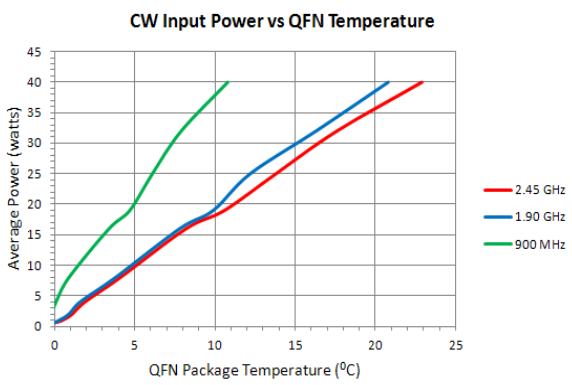
4. CW Switch Insertion Loss at +25°C



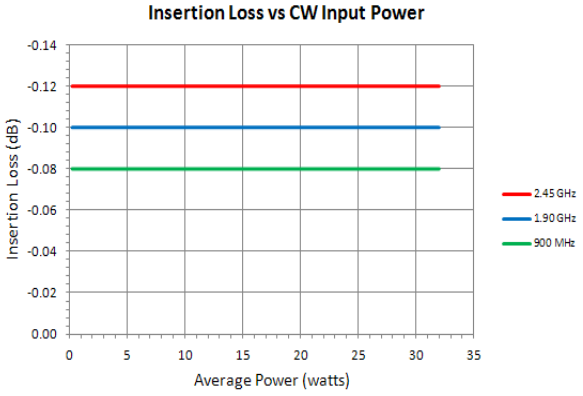


5. Switch Isolation at +25°C

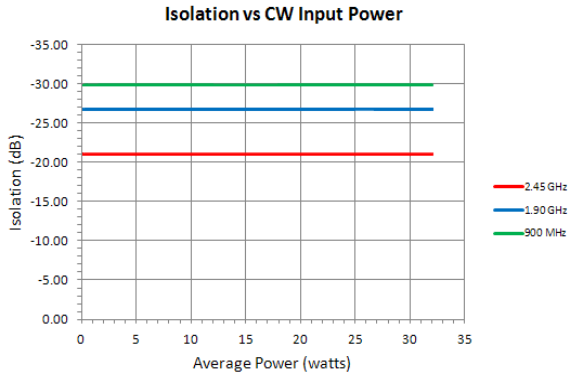
6. 3-Channel CW Input Power at +25°C



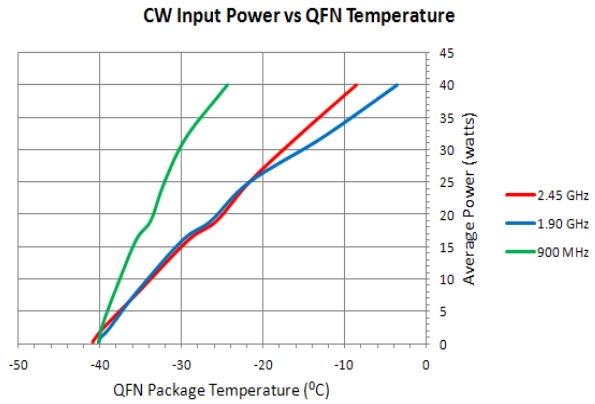
7. CW Input Power at 0°C



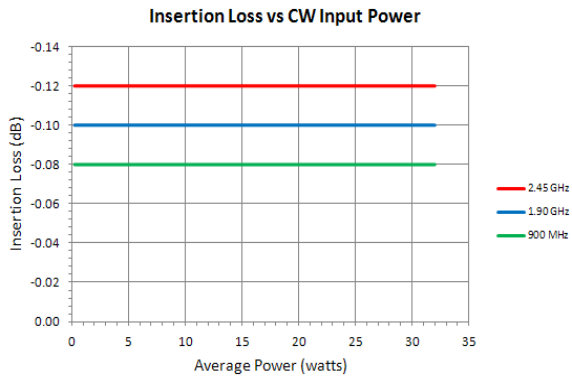
8. Switch Insertion Loss at 0°C



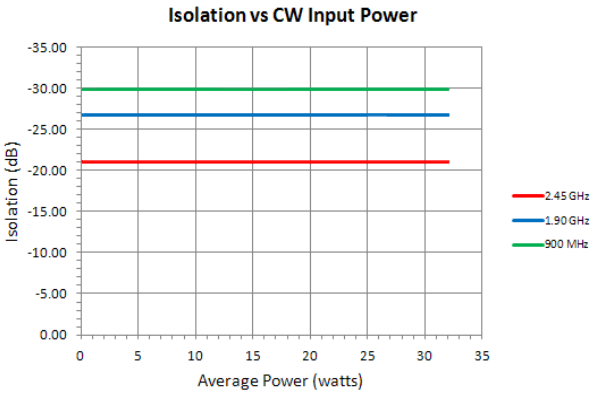
9. Switch Isolation at 0°C



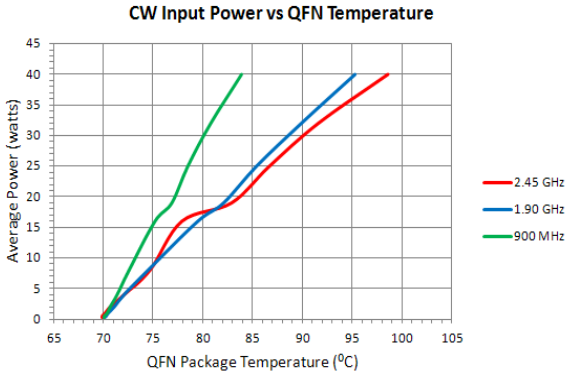
10. CW Input Power at -40°C



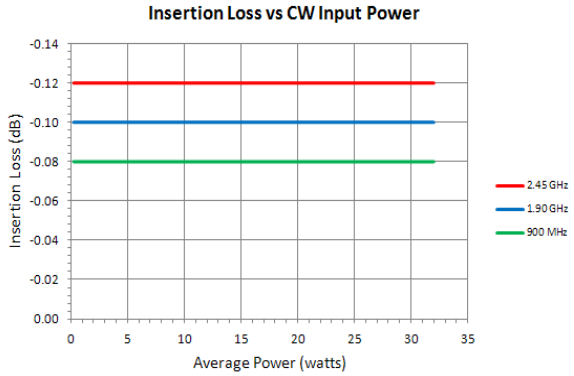
11. Switch Insertion Loss at -40°C



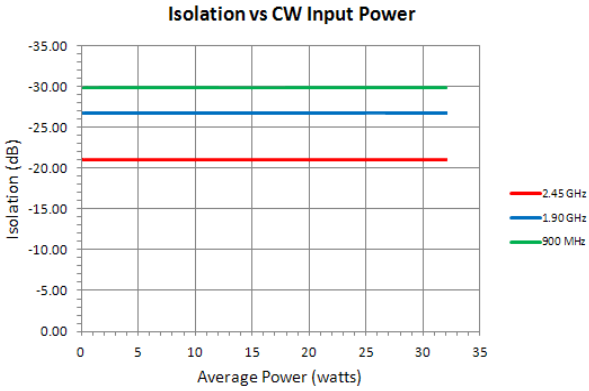
12. Switch Isolation at -40°C



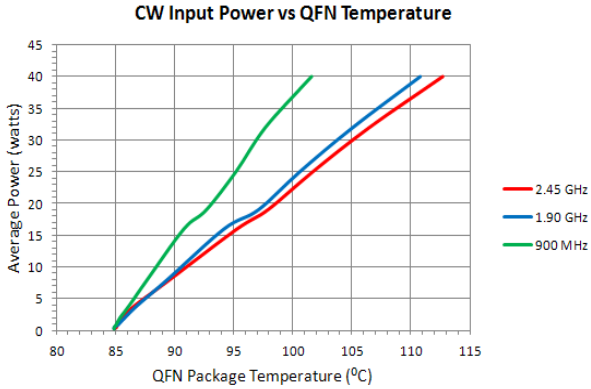
13. CW Input Power at +70°C



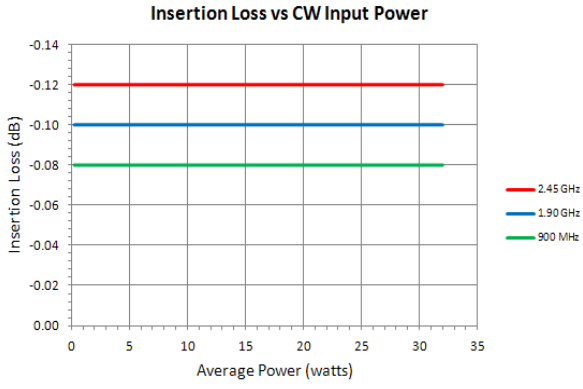
14. Switch Insertion Loss at +70°C



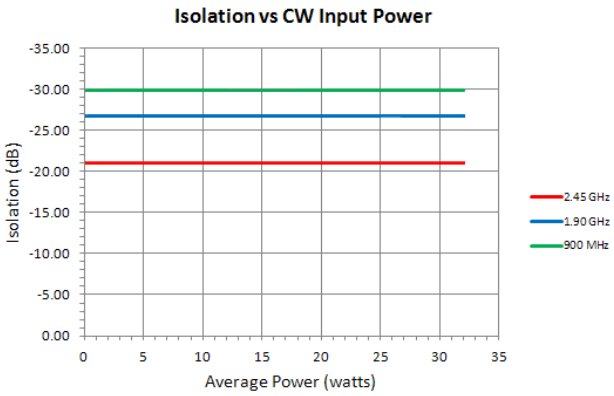
15. Switch Isolation at +70°C



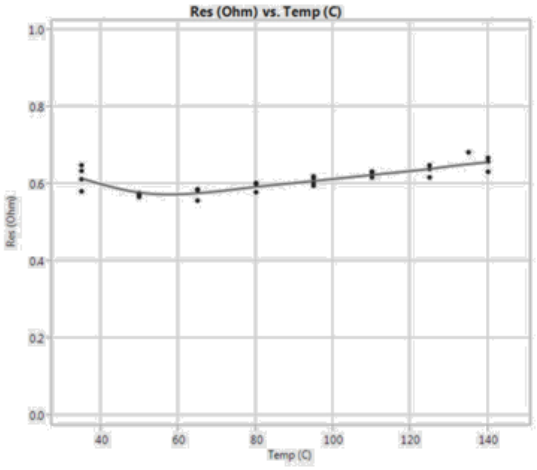
16. CW Input Power at +85°C



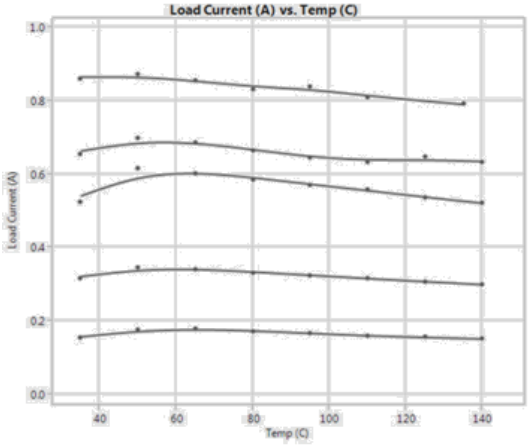
17. Switch Insertion Loss at +85°C



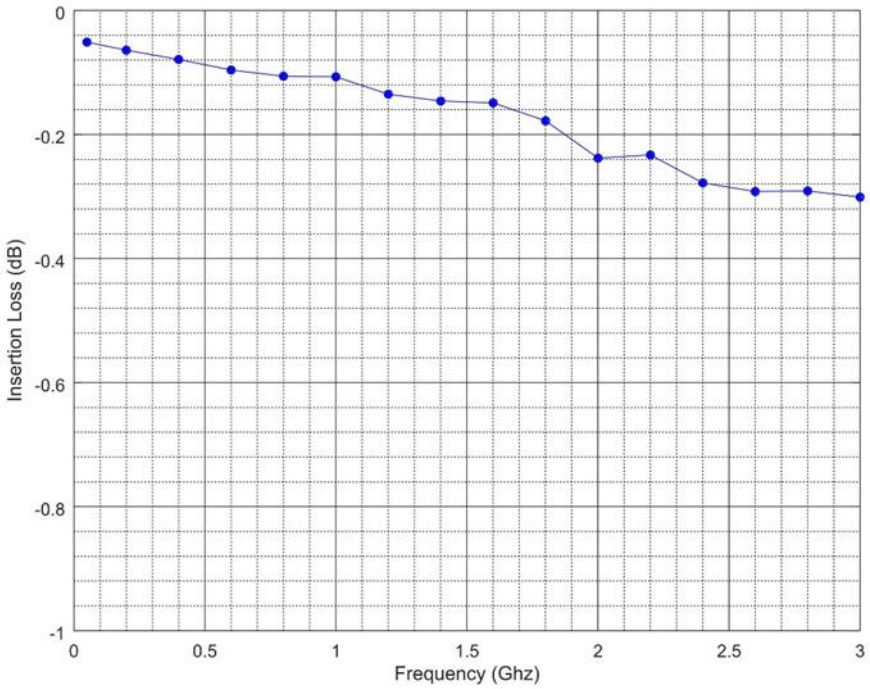
18. Switch Isolation at +85°C



19. Resistance vs Temperature



20. Load Current vs Temperature



21. Typical Channel Insertion Loss vs Frequency (S_{21})

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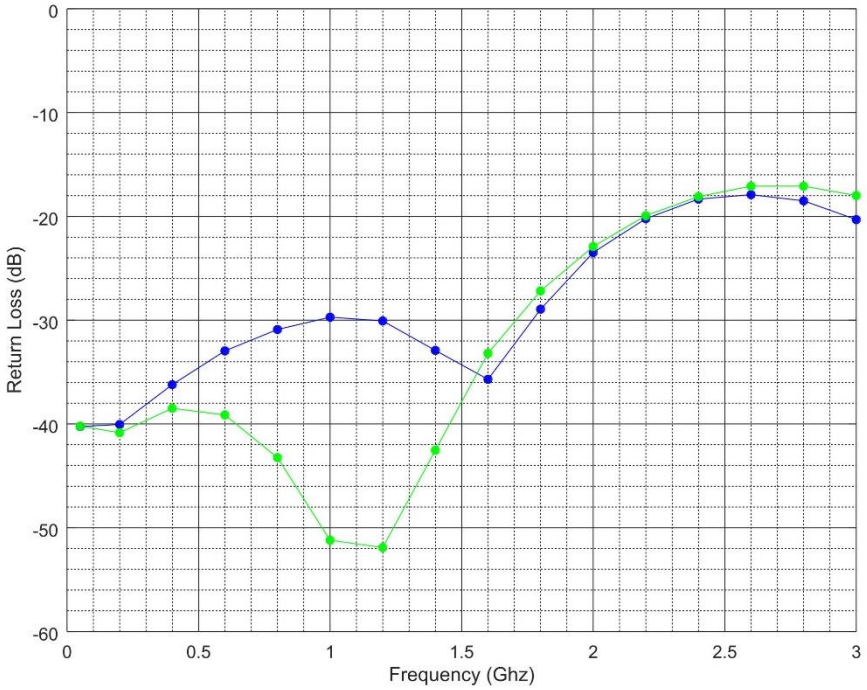
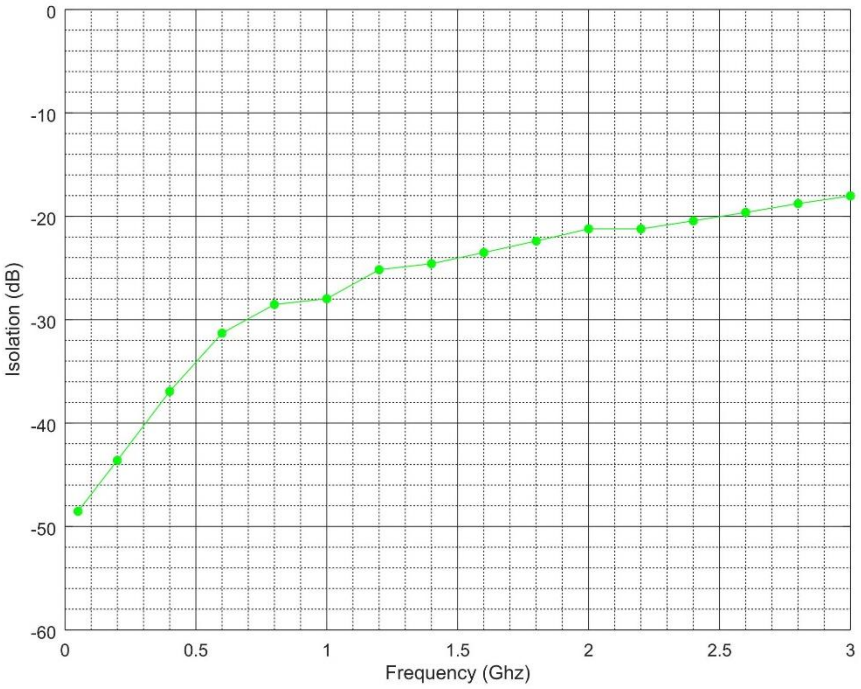


22. Typical Return Loss vs Frequency where:
Blue is at Contact / Input (S_{11}),
Green is at Beam / Output (S_{22})



23. Typical Input to Output Isolation vs Frequency (S_{21} with channel off / open)

High Voltage Gate Driver Control

Operating Description

The integrated high voltage gate driver is controlled through a serial-to-parallel interface that drives the high voltage gate lines of the switches. Switch control data is shifted into a 10-bit shift register, latched, level translated, and applied as gate control signals as shown in block diagram Figure 5 below.

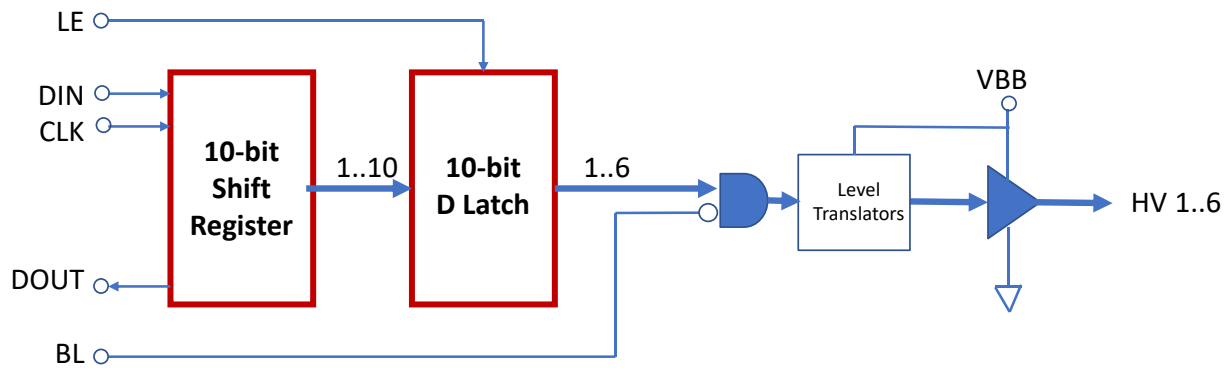


Figure 5: High Voltage Gate Driver Block Diagram

The gate driver is controlled by serial data input to DIN, sampled by CLK, latched by LE, and blanked by BL as follows:

- A 10-bit data byte is serially loaded into shift register bits 1-to-10 on the positive edge of CLK. Shift order is MSB first starting with bit 10.
- Parallel data from the shift register is transferred to the high voltage gate output buffers through a 10-bit D latch when the latch enable input LE is logically high.
- The MM3100 uses only six of the ten data bits latched for switch control. Bits 1 through 6 correspond to high voltage gate lines HV1 through HV6 respectively. Bits 7,8,9 and 10 are not used. Data bits set to logical “1” close the corresponding switch to On and “0” open the switch to Off.
- Shift register data output pin DOUT may be used to cascade multiple devices by connecting DOUT of the first device to DIN of the next device. Other control signals should be shared between all the devices. In this case it is recommended to load 10-bit words consisting of four dummy bits and six switch control bits so that each data packet controls one switch.
- There is no reset function. To clear register content, new data must be loaded.
- The blanking input BL will turn all gates off when logically high. The pin should be logically low for normal operation.

Table 6 Truth Function Table

	Inputs				Shift Register	High Voltage Output HVx
Function	Data	CLK	LE	BL	1 2…10	1 2 3 - - - - 10
All off (blank)	X	X	X	H	* *…*	L L L - - - - L
Load Shift Register	H/L	↑	L	L	H/L *…*	* * * - - - - *
Latched	X	X	L	L	* *…*	* * * - - - - *
Transfer	H/L	X	H	L	H/L *…*	H/L * * - - - - *

Note:

H = High logic level
L = Low logic level
X = Don't care logic level
↑ = Low to high logic transition
* = Dependent on the previous stage's state before the last CLK or last LE high
HVx corresponds to high voltage gate drivers where only HV1..6 are used

Package Drawing

49 Lead Ball Grid Array 0.30mm Ball, 0.50mm Pitch

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.800	1.925	2.050
A1	0.150	-	-
A2	1.650	1.725	1.800
A3	1.275	1.300	1.325
A4	0.100	-	-
A5	0.375	0.425	0.475
D	6.000 BSC		
E	6.000 BSC		
D1	5.000 BSC		
E1	4.000 BSC		
b	0.250	0.300	0.350
e	0.500BSC		

Dimensional Tol.	
aaa	0.100
bbb	0.100
ccc	0.200
ddd	0.120
eee	0.150
fff	0.080

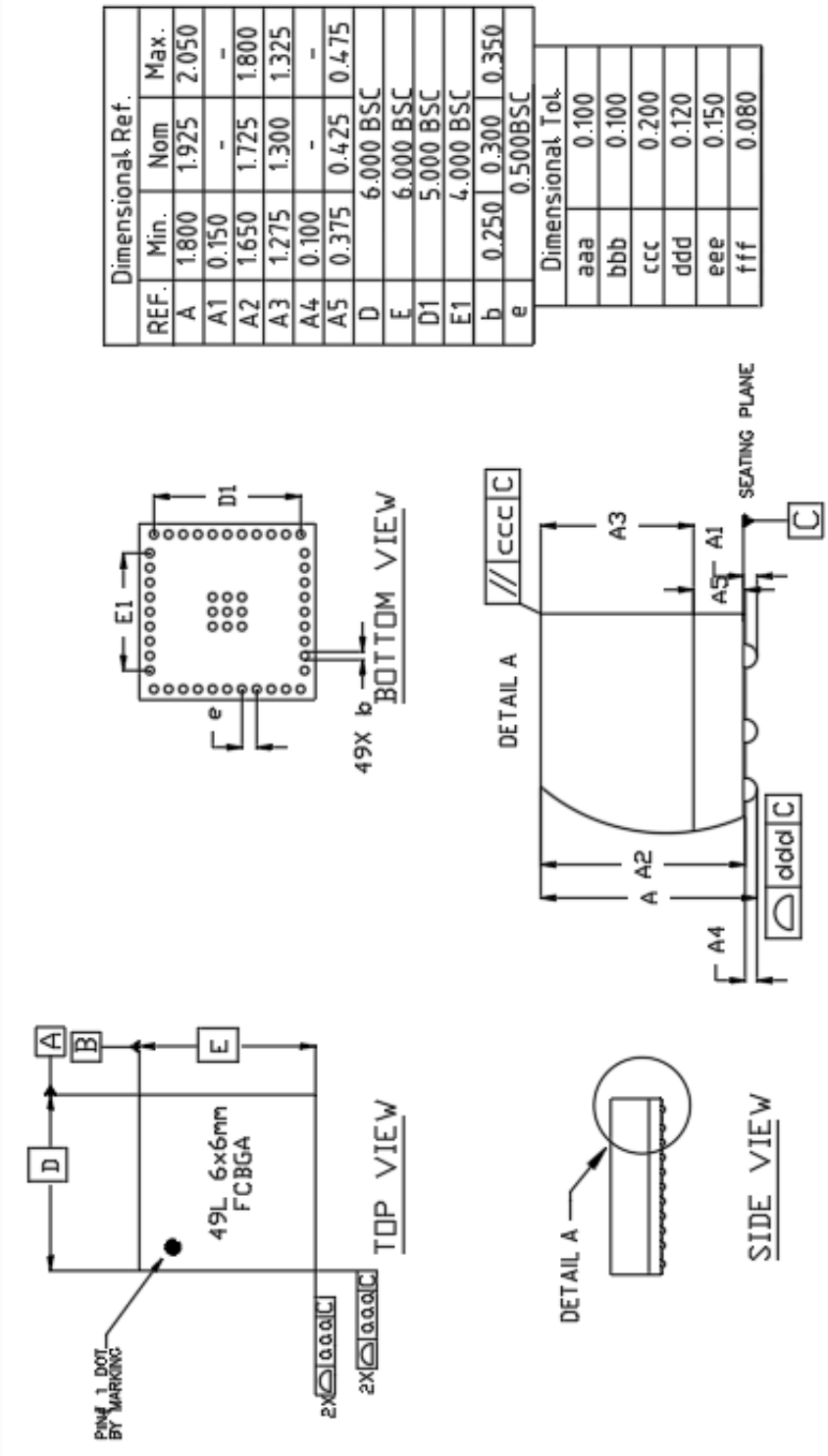


Figure 6 Package Drawing

ES France - Département RF & Hyperfréquences - 127 rue de Buzenval BP 26 - 92380 Garches
Tél. 01 47 95 99 60 - Fax. 01 47 01 16 22 - e-mail: hyper@es-france.com - Site Web: www.es-france.com

Recommended PCB Layout and SMT Parameters

- PCB lands should be as shown in the pad pattern diagram
- Connect RFG node (floating shield inside the package) to RF Signal Ground
- Open space around the package can have grounded thru holes
- ENIG (Electroless Nickel Immersion Gold) pad surface finish
- 20 micron (µm) thick solder mask
- Type 3 or higher solder paste with no clean flux
- Component placement force not to exceed 100 grams

Recommended PCB Pad Pattern

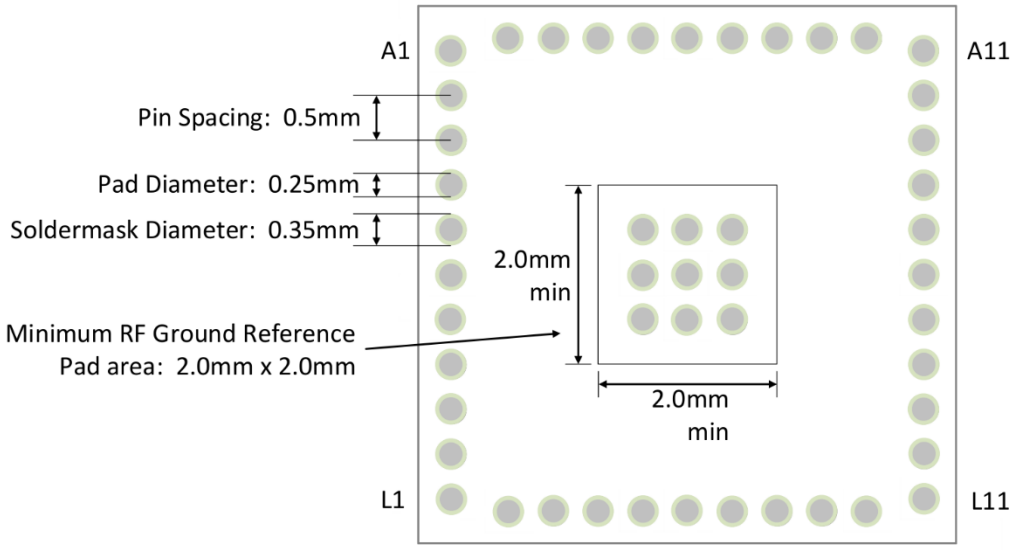


Figure 7: Recommended PCB Pad Pattern

Recommended Solder Reflow Profile

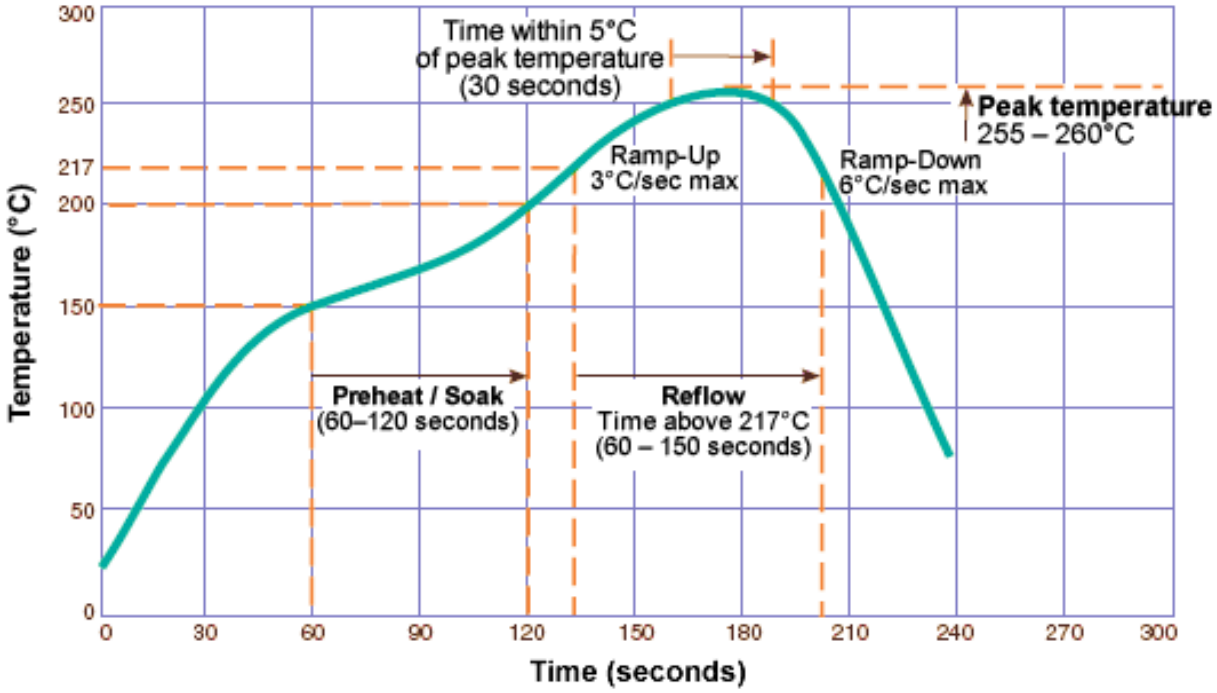


Figure 8: Reflow Profile

Follow Moisture Sensitivity Level (MSL) 3 handling precautions specified in IPC/JEDEC J-STD-020.

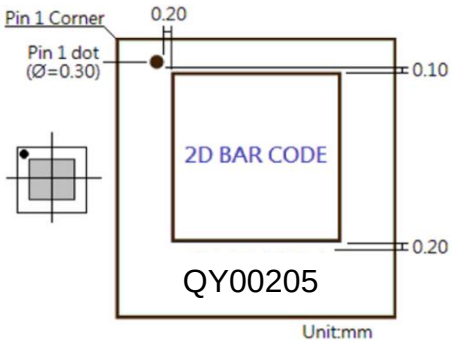
Storage and Shelf Life

Under typical industry storage conditions (≤30 °C/60% RH) in Moisture Barrier Bags:

- Customer Shelf Life: 24 months from customer receipt date
- Extended Shelf Life: 60 months from customer receipt date if re-bagged every 32 months or less.
- Floor life: Moisture Sensitivity Level (MSL) testing is not required for Hermetic package as per JESD47K.

Package Options and Ordering Information

The MM3100 package marking and nomenclature is illustrated in Figure 9 below.



Dot ● = Pin 1 Indicator
Line 1 = 2D Bar Code
Line 2 = Device Part Number

Figure 9: Package Marking Drawing

Ordering Information

Part Number	ECCN	Package	Packaging	Temp Range
MM3100-00	EAR99	6mm x 6mm x 2mm BGA	Tray	-40°C to +85°C
MM3100-EVK	EAR99	EVK	N/A	

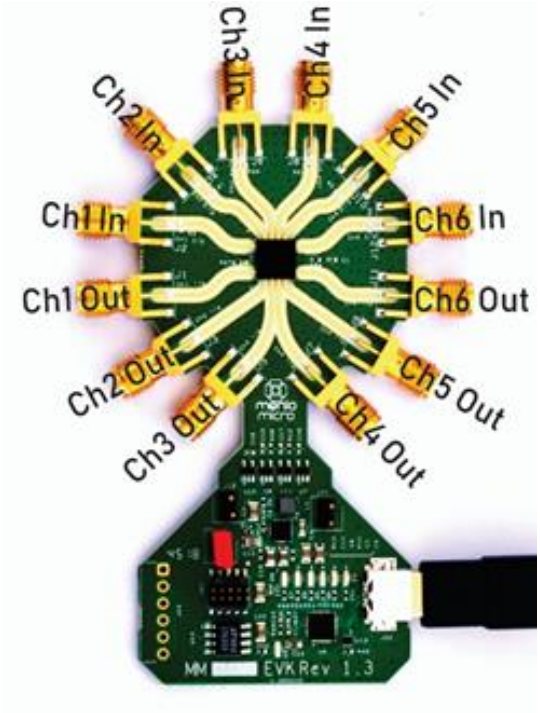


Figure 10: Evaluation Kit (EVK)

Important Information

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