



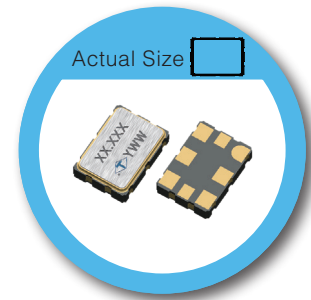
OD-M Type High Frequency and Ultra Low Noise 7.0 x 5.0mm SMD Crystal Oscillator

FEATURE

- Low Power Supply Voltage: 3.3, 2.5 and 1.8V Supply Options
- Clock Output: LVPECL, LVDS, CML, HCSL and LVCMOS
- Output Frequency Support from 15MHz to 2.1GHz
- Ultra Low Noise, Phase Jitter < 300 fs
(Typical: 150 fs at 12kHz to 20MHz Frequency Offsets)
- Tri-state Enable / Disable Mode.
- Temperature Range: -40 to 85°C
- Pb-free/RoHS Compliant

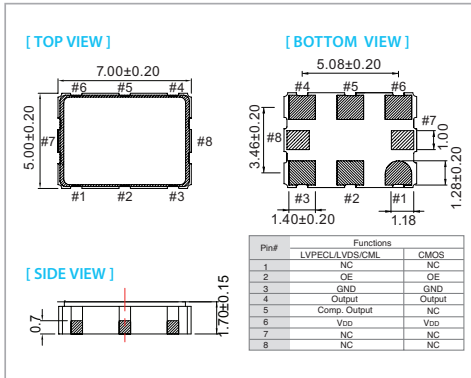
TYPICAL APPLICATION

- SONET/SDH, Gigabit Ethernet
- Storage Area Networking (SAN)
- SD/HD Video
- FPGA Clock Generation

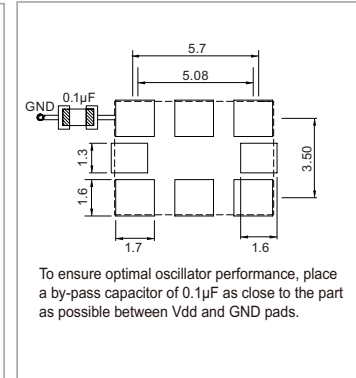


RoHS Compliant

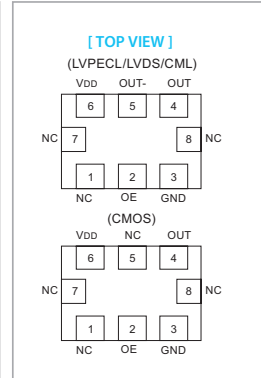
DIMENSION (mm)



SOLDER PAD LAYOUT(mm)



PIN ASSIGNMENTS



ELECTRICAL SPECIFICATION

Parameter			LVPECL				unit
			3.3V		2.5V		
			Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD) ±10%			VDD-10%	VDD+10%	VDD-10%	VDD+10%	V
Frequency Range			15	2100	15	2100	MHz
Standard Frequency			100, 106.25, 125, 156.25, 187.5, 200, 212.5, 266, 300, 312.5, 400				
Supply Current			—	110	—	95	mA
Output Level	Output High	VDD-1.165	VDD-0.8	VDD-1.165	VDD-0.8	V	
	Output Low	VDD-2.0	VDD-1.55	VDD-2.0	VDD-1.55		
Transition Time (20%-80%)	Rise Time / Fall Time	—	0.35	—	0.35	nSec	
Duty Cycle			45	55	45	55	%
Startup Time			—	8	—	8	mSec
Tri-State Mode (Input to Pin 2)	Enable	0.7 x VDD	—	0.7 x VDD	—	V	
	Disable	—	0.3 x VDD	—	0.3 x VDD		
Standby Current			—	110	—	95	mA
Phase Noise			Typ.	Max.	Typ.	Max.	
At VDD=3.3V, Fout=873.515MHz	1kHz offset	-106	—	-106	—	dBc/Hz	
	10kHz offset	-115	—	-115	—		
	100kHz offset	-123	—	-123	—		
	1MHz offset	-133	—	-133	—		
	20MHz offset	-150	—	-150	—		
RMS Phase Jitter (12kHz to 20MHz)			150	300	150	300	fs
Period Jitter			—	50	—	50	ps

Note: not all combination of options are available. Other specifications may be available upon request.

Parameter			LVDS						unit
			3.3V		2.5V		1.8V		
			Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD) ±5%			–	–	–	–	1.71	1.89	V
Supply Voltage Variation (VDD) ±10%			3.63	2.97	2.25	2.75	–	–	
Frequency Range			15	2100	15	2100	15	2100	MHz
Standard Frequency			100, 106.25, 125, 156.25, 187.5, 200, 212.5, 266, 300, 312.5, 400						
Supply Current			–	90	–	80	–	70	mA
Output Level	Output High		–	1.6	–	1.6	–	1.6	V
	Output Low		0.9	–	0.9	–	0.9	–	
Transition Time (20%-80%)	Rise Time / Fall Time		–	0.35	–	0.35	–	0.35	nSec
Duty Cycle			45	55	45	55	45	55	%
Startup Time			–	8	–	8	–	8	mSec
Tri-State Mode (Input to Pin 2)		Enable	0.7 x VDD	–	0.7 x VDD	–	0.7 x VDD	–	V
		Disable	–	0.3 x VDD	–	0.3 x VDD	–	0.3 x VDD	
Standby Current			–	90	–	80	–	70	mA
Phase Noise			Typ.	Max.	Typ.	Max.	Typ.	Max.	
At VDD=3.3V, Fout=873.515MHz		1kHz offset	-106	–	-106	–	-106	–	dBc/Hz
		10kHz offset	-115	–	-115	–	-115	–	
		100kHz offset	-123	–	-123	–	-123	–	
		1MHz offset	-133	–	-133	–	-133	–	
		10MHz offset	-150	–	-150	–	-150	–	
RMS Phase Jitter (12kHz to 20MHz)			150	300	150	300	150	300	fs
Period Jitter			–	50	–	50	–	50	ps

Parameter		CML						unit
		3.3V		2.5V		1.8V		
		Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD) ±5%		—	—	—	—	1.71	1.89	V
Supply Voltage Variation (VDD) ±10%		3.63	2.97	2.25	2.75	—	—	
Frequency Range		15	2100	15	2100	15	2100	MHz
Standard Frequency		100, 106.25, 125, 156.25, 187.5, 200, 212.5, 266, 300, 312.5, 400						
Supply Current		—	90	—	80	—	70	mA
Output Level	Output High	VDD-0.085	VDD	VDD-0.085	VDD	VDD-0.085	VDD	V
	Output Low	VDD-0.6	VDD-0.32	VDD-0.6	VDD-0.32	VDD-0.6	VDD-0.32	
Transition Time (20%-80%)	Rise Time / Fall Time	—	0.35	—	0.35	—	0.35	nSec
Duty Cycle		45	55	45	55	45	55	%
Startup Time		—	8	—	8	—	8	mSec
Tri-State Mode (Input to Pin 2)	Enable	0.7 x VDD	—	0.7 x VDD	—	0.7 x VDD	—	V
	Disable	—	0.3 x VDD	—	0.3 x VDD	—	0.3 x VDD	
Standby Current		—	90	—	80	—	70	mA
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.	
At VDD=3.3V, Fout=873.515MHz	1kHz offset	-107	—	-107	—	-107	—	dBc/Hz
	10kHz offset	-117	—	-117	—	-117	—	
	100kHz offset	-125	—	-125	—	-125	—	
	1MHz offset	-135	—	-135	—	-135	—	
	10MHz offset	-150	—	-150	—	-150	—	
RMS Phase Jitter (12kHz to 20MHz)		150	300	150	300	150	300	fs
Period Jitter		—	50	—	50	—	50	ps

Parameter		HCSL						Unit
		3.3V		2.5V		1.8V		
		Min.	Max.	Min	Max.	Min.	Max.	
Supply Voltage Variation (VDD)±10%		3.63	2.97	2.25	2.75	1.71	1.89	V
Frequency Range		15	700	15	700	15	700	MHz
Supply Current		-	115	-	100	-	94	mA
Output Level	Output High	0.66	1.15	0.66	1.15	0.66	1.15	V
	Output Low	0	0.15	0	0.15	0	0.15	V
Transition Time (20% - 80%)	Rise Time	-	0.4	-	0.4	-	0.4	nSec
	Fall Time	-	0.4	-	0.4	-	0.4	nSec
Duty Cycle		45	55		55	45	55	%
Startup Time		-	8		8	-	8	mSec
Tri-State mode (Input to Pin 2)	Enable	0.7 x VDD	-	0.7x VDD	-	0.7xVDD	-	V
	Disable	-	0.3 x VDD	-	0.3 x VDD	-	0.3 x VDD	V
Stand by Current	Disable	-	115	-	100	-	94	mA
Output Load		50 ohms to GND						
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.	
At VDD=3.3V, fout=873.515MHz	1kHz offset	-87	-	-87	-	-87	-	dBc/Hz
	10kHz offset	-110	-	-110	-	-110	-	dBc/Hz
	100kHz offset	-127	-	-127	-	-127	-	dBc/Hz
	1MHz offset	-138	-	-138	-	-138	-	dBc/Hz
	10MHz offset	-153	-	-153	-	-153	-	dBc/Hz
RMS Phase Jitter (12KHz to 20MHz)		150	300	150	300	150	300	fs
Period Jitter		-	50	-	50	-	50	ns

Note: not all combination of options are available. Other specifications may be available upon request.

Parameter		CMOS						unit
		3.3V		2.5V		1.8V		
		Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD) ±5%		—	—	—	—	1.71	1.89	V
Supply Voltage Variation (VDD) ±10%		3.63	2.97	2.25	2.75	—	—	
Frequency Range		15	250	15	250	15	250	MHz
Supply Current		—	90	—	80	—	70	mA
Output Level	Output High	0.9 x VDD	—	0.9 x VDD	—	0.9 x VDD	—	V
	Output Low	—	0.1 x VDD	—	0.1 x VDD	—	0.1 x VDD	
Transition Time (20%-80%)	Rise Time / Fall Time	—	1.2	—	1.5	—	2	nSec
Duty Cycle	Fout <100MHZ	45	55	45	55	45	55	%
	Fout >100MHZ	40	60	40	60	40	60	
Startup Time		—	8	—	8	—	8	mSec
Tri-State Mode (Input to Pin 2)	Enable	0.7 x VDD	—	0.7 x VDD	—	0.7 x VDD	—	V
	Disable	—	0.3 x VDD	—	0.3 x VDD	—	0.3 x VDD	
Period Jitter		—	100	—	100	—	100	mA

FREQ. STABILITY vs. TEMP. RANGE

Temp. (°C) \ ppm	±20	±25	±30	±50
-20~+70	△	○	○	○
-40~+85	X	△	○	○

* ○: Available △: Conditional X: Not available

* Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration

Note: not all combination of options are available. Other specifications may be available upon request.