MM1205

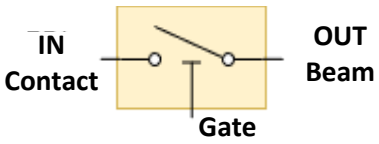
6 Channel SPST High Frequency Signal Relay

Product Overview

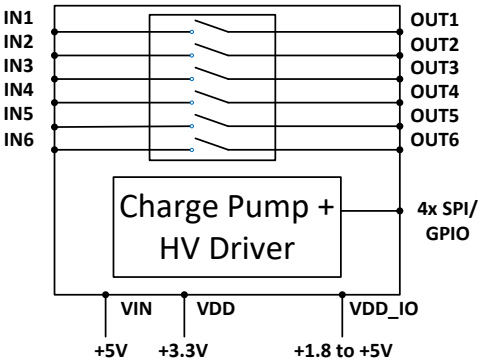
Description

The MM1205 device is a 6-channel SPST High Frequency Signal Relay intended for signal switching applications for DC, analog, and RF circuits. Each channel provides low on-state contact resistance and insertion loss, high off-state isolation from DC to over 3 GHz with industry-leading cycle life. The flexibility of six SPST channels enables implementation of different signal topologies such as dual SP3T, triple SP2T, or a 2 x 3 matrix. The MM1205 features an integrated driver and control logic circuit with SPI and GPIO interface control options, along with integrated charge pump to drive the gate. The device only requires 3.3 V and 5 V external supplies to operate. Each channel can be individually controlled, and multiple devices can be daisy-chained together.

Features



- 1.0 A per channel
- 2.0 A per package
- Input to output isolation > 10 GΩ, typical
- Low on-state resistance 1.0 Ω typical (per channel)
- DC carry voltage up to 38 V



- Operation from DC to 3 GHz
- 25 W (CW) to 300 MHz, 200 W (pulsed) power handling
- Low on-state insertion loss, 0.5 dB @ 3.0 GHz, typical
- 17 dB input to output off-state isolation @ 3.0 GHz, typical

- Integrated driver and charge pump
- High reliability 3 billion switching operations, typical
- 8 mm x 8 mm LGA package

Applications

- High Density Switch Matrices
- Automated Test and Measurement Systems
- High-Power Tunable Resonators and Filters
- Broadband Power Amplifier Impedance Matching
- Electronically Steerable Antennas and Phase Shifters
- Mechanical, Reed, and Photo Relay Replacement

Markets

- Test & Measurement
- Wireless Charging
- Scientific and Medical
- Telecom

Electrical Specifications

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM1205 should be restricted to the recommended operating conditions listed in Table 2.

Electrostatic Discharge (ESD) Safeguards

The MM1205 is a Class 0 ESD device. When handling the MM1205, observe precautions as with any other ESD sensitive device. Do not exceed the voltage ratings specified in Table 1.

Power Sequencing

When using the internal charge pump, there are no power sequencing requirements for V_{IN}, V_{DD}, or V_{DD_IO} supplies.

When using an external high voltage, apply V_{DD}, and V_{DD_IO} supplies before applying high voltage to V_{PP}. This requires V_{IN} is connected to CPGND and CP_EN is NC or connected to GND,

Table 1. Absolute Maximum Ratings[1]

Parameter	Minimum	Maximum	Unit
Driver Voltage Supply (V_{DD})	-0.3	3.6	V
I/O Supply Voltage (V_{DD_IO})	-0.3	5.5	V
Charge Pump Input (V_{IN})	-0.3	5.5	V
Logic Input Levels	-0.3	V_{DD_IO} + 0.3	V
On-State DC Carry Voltage:			
Internal Charge Pump[2]	0	30	V
External 100 V to V_{PP}[3]	0	38	V
Off-State Output Voltage to GND[4]	0	50	V
Off-State Voltage INx to OUTx[5]	-100	100	V
DC Carry Current / Channel[6]	—	1.0	A
Total Carry Current per Device[6]	—	2.0	A
Storage Temperature Range[7]	-65	+150	ºC
ESD Rating HBM V_{PP} Pin	—	500	V
ESD Rating HBM Control and Power Pins[8]	—	2000	V
ESD Rating HBM Channel I/O Pins[9, 10]	—	100	V
Mechanical Shock[11]	—	500	G
Vibration[12]	—	500	Hz

Notes:

1. All parameters must be within recommended operating conditions. Maximum DC and AC power can only be applied in the on-state.
2. Voltage allowed on the output to prevent unintended de-actuation when using the internal charge pump.
3. Voltage allowed on the output to prevent unintended de-actuation when providing an external 100 V to the V_{PP} pin.
4. Voltage on the output of a given channel to prevent unintended actuation.
5. This also applies to ESD events.
6. See section Thermal and Power Handling Considerations for more information.
7. See section Storage and Shelf Life for more information on shelf and floor life.
8. Control and power pins include: V_{IN}, V_{DD}, V_{DD_IO}, FLT_MODE, FLTB, FLIP_BIT, CP_EN, MODE, SCK, MOSI, MISO, SSB, and CTL1-4.
9. Channel I/O pins include: IN1 to IN6, OUT1 to OUT6.
10. IN and OUT pins must not be allowed to electrically float during channel operation. See section Floating Node Restrictions for details on avoiding floating nodes.
11. See JESD22-B104 for mechanical shock test methodology at 1.0 ms, half-sine, 5 shocks/axis, 6 axis.
12. See JESD22-B103 for vibration test methodology at 3.1G and 30 min/cycle, 1 cycle/axis, 3 axis.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Charge Pump Power Supply	V_{IN}	4.85	5.5	V
Low Voltage Digital Supply	V_{DD}	3.0	3.6	V
Logic Reference Level	V_{DD_IO}	1.71	5.25	V
Ambient Temperature Range	T_A	-40	85	ºC
Case Temperature	T_C	—	+125	ºC
SPI Clock Frequency	f_{SCK}	—	33	MHz
Switch Cycle Frequency		—	100	Hz

Electrical Characteristics

All specifications valid over full supply voltage and operating temperature range unless otherwise noted.

Table 3a. DC and Analog Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
On / Off Switching and Settling Time[1]				
Turn on time (t_{ON})	—	16.5	—	µs
Turn off time (t_{OFF})	—	7	—	µs
On / Off Channel Operations[2] (Cold Switched)	—	$3x10^9$	—	Cycles
On/Off Channel Operations[3] (Hot Switched)				
2 V (at 28 mA)	—	$7x10^8$	—	Cycles
3 V (at 42 mA)	—	$1.5x10^8$	—	Cycles
4 V (at 56 mA)	—	$1.5x10^7$	—	Cycles
5 V (at 70 mA)	—	$1.5x10^6$	—	Cycles
Off-State Input-Output Leakage @ 30V[4]	—	250	—	fA
On-State Resistance[5]	—	1.0	1.5	Ω
Off-State Capacitance (C_{Off})[6]	—	45	—	fF
Channel to Channel Off-State Capacitance (C_{Ch-Ch})[7]				
In1 – In2	—	50	—	fF
In1 – In6	—	2	—	fF
Video Feedthrough[8]	—	5	—	mV_{PK-PK}

Notes:

1. Measured from 50% rising edge of final SSB to settling within 0.05dBm of final value.
2. Predicted number of operation cycles, measured at 10 kHz cycling rate, at room temperature with Hot Switch Restrictions.
3. Point at which 50% of the population of tested channels failed. Hot switched operations measured at room temperature with a 71.5 Ω load. See Figure 15 in section Switch Reliability Test Results.
4. Device measured on probe station. For performance over voltage see Figure 9.
5. Measured at 1 A, DC.
6. Capacitance between input and output pins measured at 1 MHz at 25°C ambient.
7. Capacitance between channel inputs measured at 1 MHz at 25°C ambient.
8. Performed with 50 Ω terminations on all input and output channels

All specifications valid over full supply voltage and operating temperature range with operating frequency range of DC to 3.0 GHz unless otherwise noted.

Table 3b. RF Electrical Characteristics

Parameter	Minimum	Typical	Max	Unit
CW Power / Channel [1, 2]	—	—	25	W
Peak Power / Channel @ 10% Duty Cycle [3]	—	—	200	W
Insertion Loss @ 3.0 GHz	—	0.5	—	dB
Input / Output Return Loss @ 3.0 GHz	—	14	—	dB
Input to Output Isolation @ 3.0 GHz	—	17	—	dB
Adjacent Channel Isolation @ 3.0 GHz [4]				
Adjacent Channel Closed	—	20	—	dB
Adjacent Channel Open	—	22	—	dB
Third-Order Output Intercept (IP3)	—	85	—	dBm
Second Harmonic (H2) [5]	—	-120	—	dBc
Third Harmonic (H3) [5]	—	-120	—	dBc
Charge Pump Clock Feed Thru[6]	—	-125	—	dBm

Notes:

1. Maximum allowable Continuous Wave Power below 2.0 MHz is 1.0 W.
2. 25 W measured at 1 GHz.
3. Duty Cycle based on 10 µs period, room temperature ambient test condition.
4. See section Adjacent Channel Isolation for more information regarding isolation measurements.
5. Measured at 2.0 GHz fundamental frequency and 35 dBm input power.
6. Measured on Agilent E4440A Spectrum Analyzer with 0 dB internal attenuation, internal amplifier ON, single sweep, VBW 10 Hz, RBW 10 Hz, all I/O channels closed, at room temperature.

Table 4. Power Supply Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Charge Pump Power Supply	V_{IN}	4.85	5.0	5.5	V	
V_{IN} Current (Dynamic)[1]	I_{VIND}	—	1.7	2.75	mA	SPI mode, All CH switching at 100Hz
V_{IN} Quiescent Current	I_{VINQ}	—	1.65	2.25	mA	Charge Pump On, All I/O and Channels Static
Low Voltage Logic Supply	V_{DD}	3.0	3.3	3.6	V	
V_{DD} UVLO Rising Threshold	$UVLO_{RISE}$	2.77	—	2.95	V	
V_{DD} UVLO Falling Threshold	$UVLO_{FALL}$	2.72	—	2.90	V	
Low Voltage Digital Current[1]	I_{DD}	—	520	700	µA	SPI mode, All CH Switching at 100Hz
Low Voltage Digital Quiescent Current	I_{DDQ}	—	480	550	µA	Charge Pump On, All I/O & Channels Static
Low Voltage Digital Sleep Mode Current	$I_{DDSLEEP}$	—	<1	10	µA	Charge Pump Off, SPI and Inputs in Static State
Logic Reference Level	V_{DD_IO}	1.71	—	5.25	V	
I/O Logic Supply Current	I_{DD_IOQ}	—	<10	50	uA	All Channels Switching at 100Hz

Notes:

1. Specification is obtained by characterization.

Table 5. Digital Interface AC and DC Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Logic I/O Level High	I/O_{VH}	0.7 x V_{DD_IO}	—	V_{DD_IO}	V	
Logic I/O Level Low	I/O_{VL}	0	—	0.3 x V_{DD_IO}	V	
Logic I/O Hysteresis (SCK only)	I/O_{VH}	—	0.25	—	V	
MISO Load Capacitance[1]	C_{MISO}	—	—	10	pF	
MISO Source Current @ V_{DD_IO}:	I_{MISOH}					V_{OUT} = 0.8 x V_{DD_IO}
5 V		180	290	—	mA	
3.3 V		75	140	—	mA	
1.8 V		20	35	—	mA	
MISO Sink Current @ V_{DD_IO}:	I_{MISOL}					V_{OUT} = 0.2 x V_{DD_IO}
5.0 V		140	260	—	mA	
3.3 V		65	140	—	mA	
1.8 V		20	40	—	mA	
Pull down resistor at MOSI, SCK, SSB, CP_EN, FLIP_BIT, MODE, and FLT_MODE pins	R_{PD}	120	200	280	kΩ	SSB pull down is only in GPIO mode
CP_EN pin toggle low time	T_{TOGGLE}	500	—	—	ns	Minimum time CP_EN has to be held low to restart the IC from fault condition
FLTB pin max sink current		65	140	—	mA	FLTB = GND V_{DD_IO} = 3.3 V

Notes:

1. MISO load capacitance = input capacitance of SDI pin + trace capacitance from SDO to SDI

Table 6. Digital Interface Timing Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
SDI Valid to SCK Setup Time[1]	t_{SU}	2	—	—	ns	
SDI Valid to SCK Hold Time[1]	t_{HD}	5	—	—	ns	
SCK High Time[1]	t_{HI}	15.5	—	—	ns	
SCK Low Time[1]	t_{LO}	15.5	—	—	ns	
SSB Pulse Width[1]	t_{CSH}	15	—	—	ns	
LSB SCK to SSB High[1]	t_{CSHLD}	15	—	—	ns	
SSB Low to SCK High[1]	t_{CSSU}	15	—	—	ns	
MISO Propagation Delay from SCK Falling Edge[1]	t_{MISOH}	10	—	—	ns	
MISO Output Valid after SSB Low[1]	t_{CMISO}	20	—	—	ns	
SSB Inactive to MISO High Impedance[1]	t_{MISOZ}	—	—	10	ns	

Notes:

1. Specification is obtained by characterization.

See Programming section for driver interface timing diagrams and details.

Table 7. Driver Interface Timing Specifications

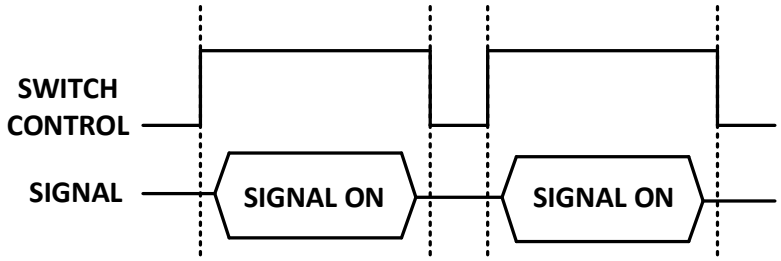
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Power-On-Reset[1]	POR	—	1.25	2.5	ms	Time for logic input signals to be considered valid after application of V_{IN} and V_{DD}.
Start-Up Time	T_{ST}	—	20	33	ms	CP_EN=1 (CPEN bit=1) to V_{PP} rises to 90% of set value

Notes:

1. Specification is for design guidance only.

Hot Switch Restrictions

For full operating lifetime, it is recommended to switch with less than 0.5 V difference between the input and output. In addition, keep the voltage on the output below 15 V when closing the switch.



If the MM1205 is used in hot switching applications, the number of cycling operations of the device will be degraded. See section Switching Reliability Test Results and Figure 15 for more information.

Floating Node Restrictions

IN/OUT pins must not be allowed to electrically float during switch operation and therefore require some form of DC path to ground to prevent charge accumulation. See Menlo Micro application note ***Avoiding Floating Nodes*** for a detailed explanation of the hazard conditions to avoid and recommended solutions. The EVK application circuit is another good example of how to avoid floating nodes.

Typical Design Considerations

Note: V_{BB} is defined as V_{PP} - V_{OUTPUT}.

When using the MM1205, exercise care to maintain certain voltage levels on the switch, depending on its state.

- To avoid **Hot Switching** when opening or closing the switch, the MM1205 Input and Output always need to be within 0.5V of each other. See section Hot Switch Restrictions for more details.
- To avoid **unintended de-actuation** of a closed switch, the voltage on the output can be no greater than the 'On-State DC Carry Voltage'.

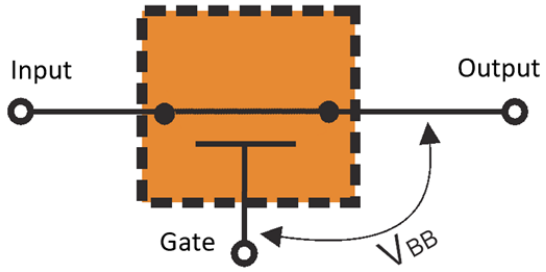


Figure 1. Closed Switch Gate (V_{BB}) to Output Voltage Considerations

- To avoid **unintended actuation** of an open switch, the output must be kept below the 'Off-State Output Voltage to GND'.
- To ensure that the switch is able to actuate, the voltage on the output must be kept below 15 V when closing the switch.

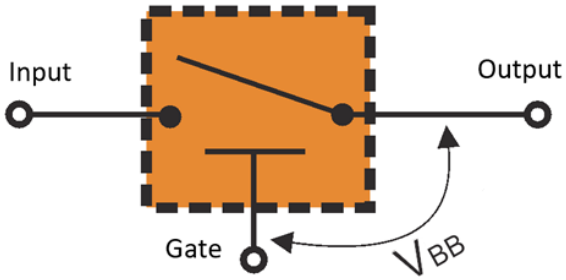


Figure 2. Open Switch Gate (V_{BB}) to Output Voltage Considerations

Thermal and Power Handling Considerations

It is recommended that the case temperature (T_C) of the MM1205 not exceed 125˚C. The rise in case temperature can be calculated using the power dissipated by the device and the thermal resistance.

$$\text{Power Dissipated } (P_D) = R_{ON} * I_L^2$$

Using the dissipated powers, the case temperature rise can be calculated.

$$\text{Case Temp Rise} = P_D * \Theta_{CA}$$

Where Θ_{CA}=46˚C/W.

A convenient graph of Case Temperature Rise versus Power Dissipated is shown in Figure 3 below.

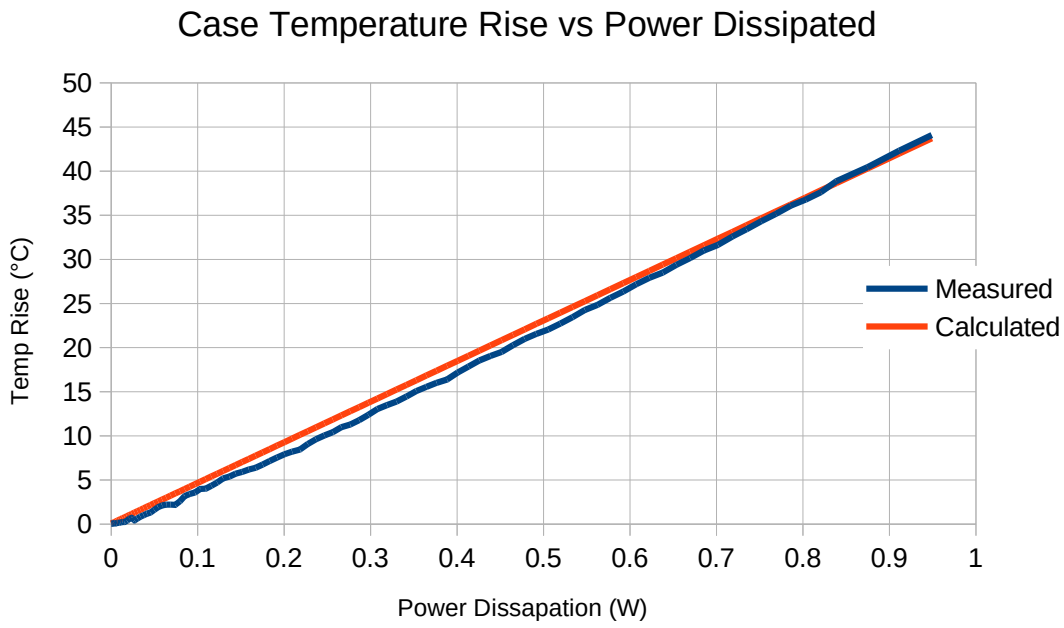


Figure 3. Case Temperature Rise versus Power Dissipated

Functional Block Diagram

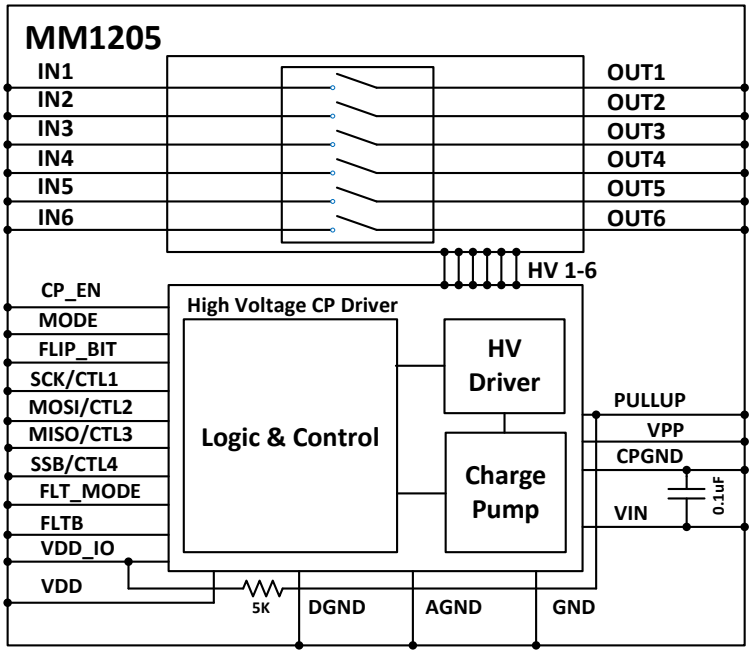


Figure 4. Functional Block Diagram (INx = Contact, OUTx = Beam)

Package/Pinout Information

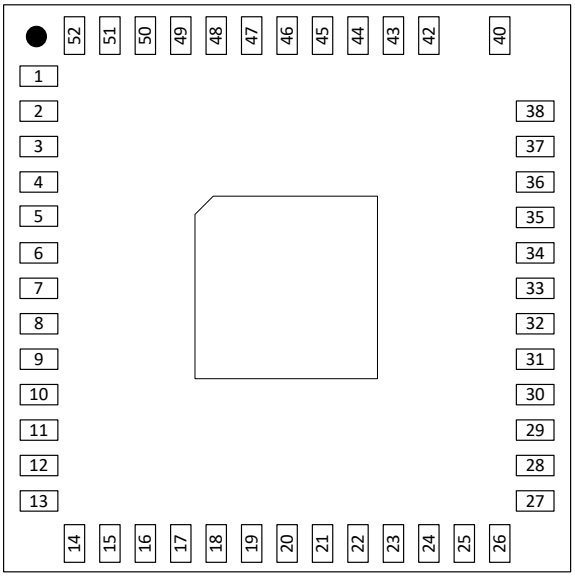


Figure 5. 52-Lead LGA (Top View)

See Table 8 for detailed pin description.

Table 8. Detailed Pin Description

Pin Name	Pin #	Description
		GND Pins
GND	2, 3, 7, 12, 14,16, 18,20, 22, 24, 42, 44, 46, 48,50,52,	Connect to common ground. These pins are internally connected to the signal ground reference.
AGND	28	Analog ground, should be connected to PCB ground.
CPGND	29	Charge pump ground, should be connected to PCB ground.
DGND	30	Digital ground, should be connected to PCB ground.
		Power Pins
V_{PP}	40	High-voltage output pin, 95V nominal when using internal charge pump. High-voltage input pin if using external high-voltage. Must connect with a 4.7 nF, 200 V, 10 % C0G ceramic capacitor to AGND. Ensure load is greater than 20MΩ.
V_{IN}	27	Connect to 5V power supply. Bypass with a low ESR 1 µF ceramic capacitor.
V_{DD}	36, 37	3.3V nominal input to digital logic and internal level translators. Bypass with a low ESR 1 µF ceramic capacitor.
V_{DD_IO}	38	For 3.3V nominal digital I/O levels, connect to V_{DD}. For alternate I/O levels, connect to a separate supply (+1.8V to +5.0V). Bypass with a low ESR 1 µF ceramic capacitor if separate from V_{DD}.
		I/O Pins
IN1	43	CH1 Input
IN2	45	CH2 Input
IN3	47	CH3 Input
IN4	49	CH4 Input
IN5	51	CH5 Input
IN6	1	CH6 Input
OUT1	23	CH1 Output
OUT2	21	CH2 Output
OUT3	19	CH3 Output

Pin Name	Pin #	Description
OUT4	17	CH4 Output
OUT5	15	CH5 Output
OUT6	13	CH6 Output
		Digital Pins
MODE	4	Logic level input to switch inputs between SPI and GPIO modes. Connect MODE to GND to select SPI mode. Connect MODE to V_{DD_IO} to select GPIO mode.
FLT_MODE	5	Fault Mode select in GPIO mode. Pull to V_{DD_IO} to disable Fault Mode. Has a built-in pull-down resistor. Pin is ignored in SPI mode.
FLIP_BIT	6	This pin has an internal pull-down resistor. In SPI mode, spread spectrum is enabled. In GPIO mode FLIP_BIT controls the logic mapping between CTL1-4 and SW1-6. For channel control, refer to Table 9.
FLTB	25	Fault indicator in GPIO and SPI modes. Open drain output to allow "Wire-OR" of multiple ICs. Goes low when a fault is detected. Can be left open if not used. Pull-up voltage must be ≤ V_{DD_IO}.
PULL-UP	26	FLTB pull up resistor configuration pin. To use the internal pull-up resistor, connect it to FLTB. If you use multiple ICs on the same PCB, an external resistor of 1K can be used to pull up to V_{DD_IO} by connecting all of the PULL_UP pins together, and then connecting them to the external resistor.
SCK/CTL1	31	Clock input in SPI mode; in GPIO mode refer to Table 9 for channel control. Has an internal pull-down resistor.
MOSI/CTL2	32	SPI data input in SPI mode; in GPIO mode refer Table 9 to for channel control. Has an internal pull-down resistor.
MISO/CTL3	33	SPI data output in SPI mode; in GPIO mode refer Table 9 to for channel control. Has an internal pull-down resistor.
SSB/CTL4	34	Chip select in SPI mode; in GPIO mode refer to Table 9 for channel control. Has an internal pull-up resistor in SPI mode, and an internal pull-down resistor in GPIO mode.
CP_EN	35	Charge pump enable pin in GPIO mode. Pull-up to V_{DD} to enable the charge pump. Has a built-in pull-down resistor. Pin is ignored in SPI mode.
		No Connect Pins
No pad	39,41	
NC	8,9,10,11	Do not connect, keep pad floating.

Performance

Typical device performance measured on MM1205.

Adjacent Channel Isolation

Adjacent channel (Ch) isolation is defined for the MM1205 in two ways:

1. Adjacent channel closed: measured between Ch 3 Output and Ch 4 input. This particular combination is the worst case for channel-to-channel isolation.
2. Adjacent channel open: measured between Ch 3 Output and Ch 4 input, with Ch 3 Closed and Ch 4 open.

Measurements are done at 3.0 GHz with a calibrated VNA and all ports terminated with 50Ω during measurement as shown in Figure 6.

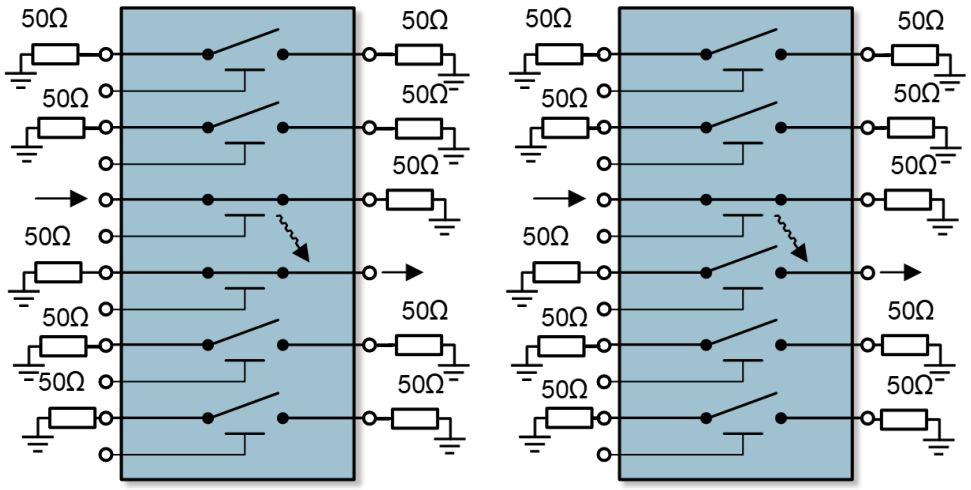


Figure 6. Adjacent Channel Isolation Measurement

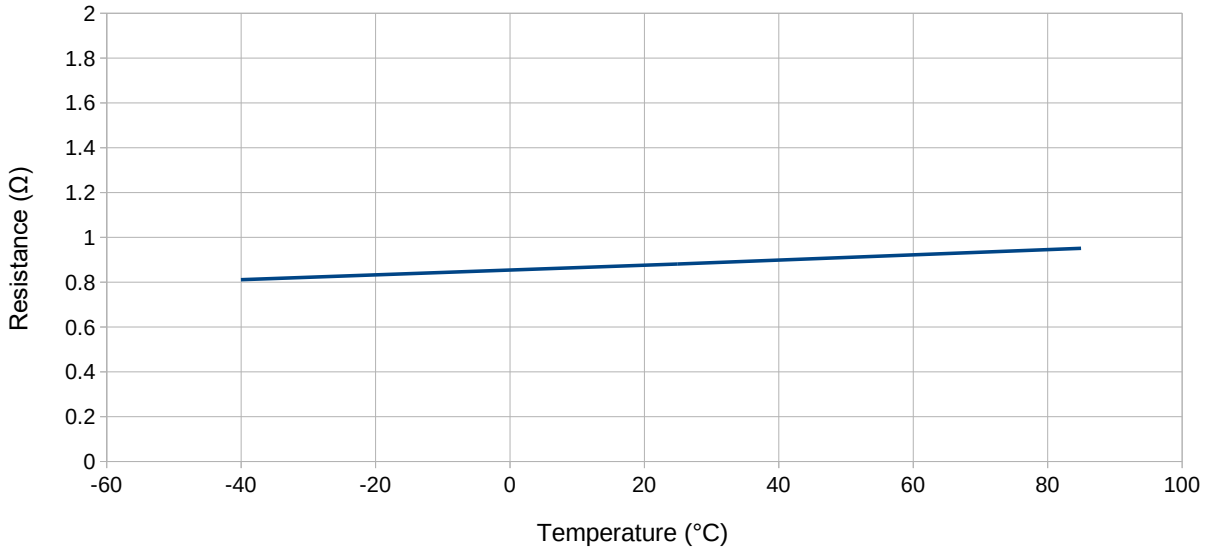


Figure 7. On-State Resistance over Temperature (Measured at 1A)

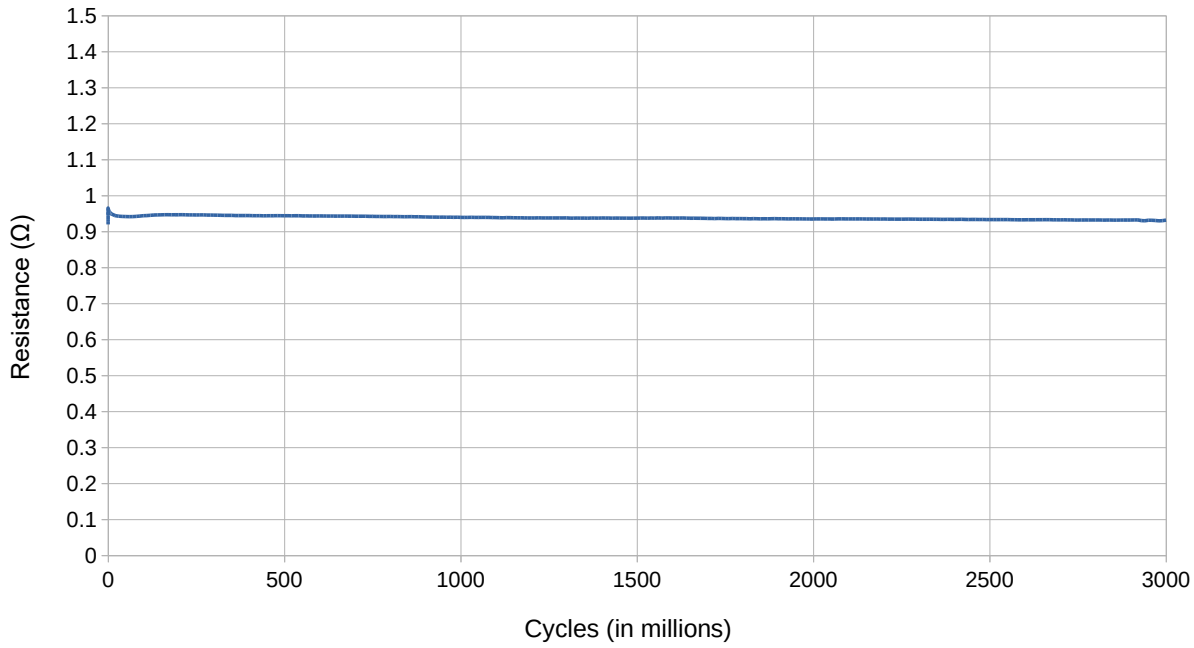


Figure 8. On-State Resistance over Cycling (Measured at 1V, 10mA Hot Switch @ 25°C)

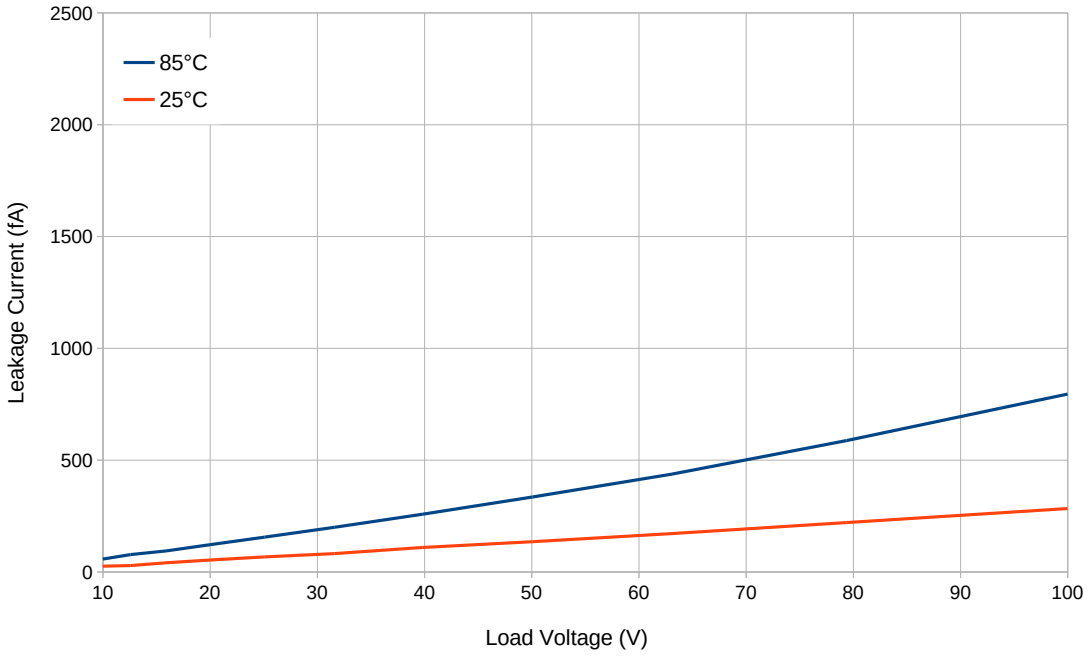


Figure 9. Off-State Input-Output Leakage Current vs V_{OFF}

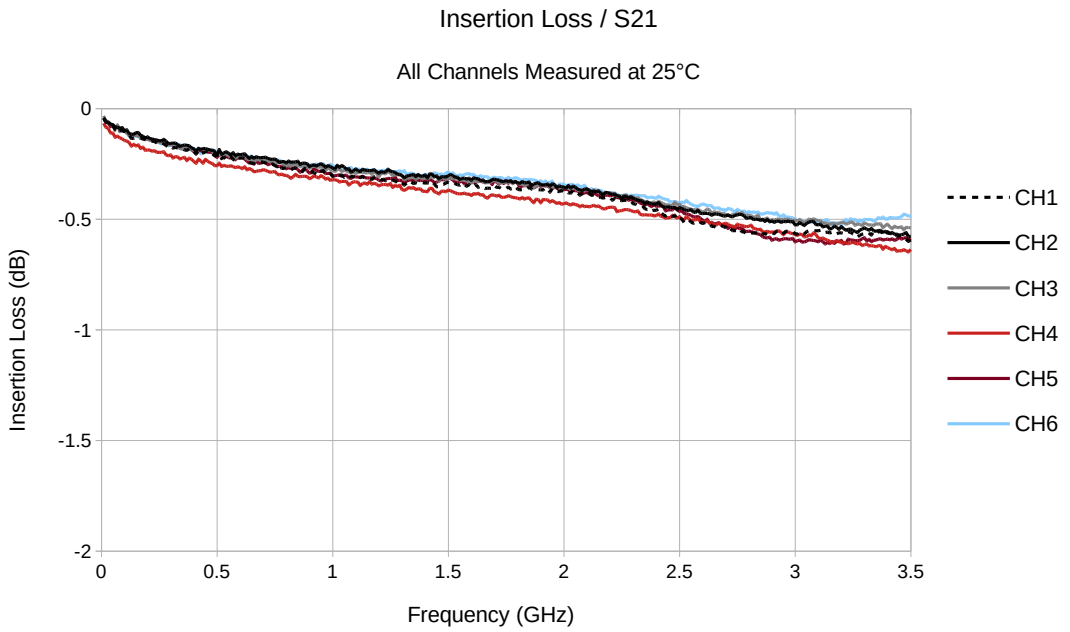


Figure 10. Typical Channel Insertion Loss vs Frequency (S_{21})

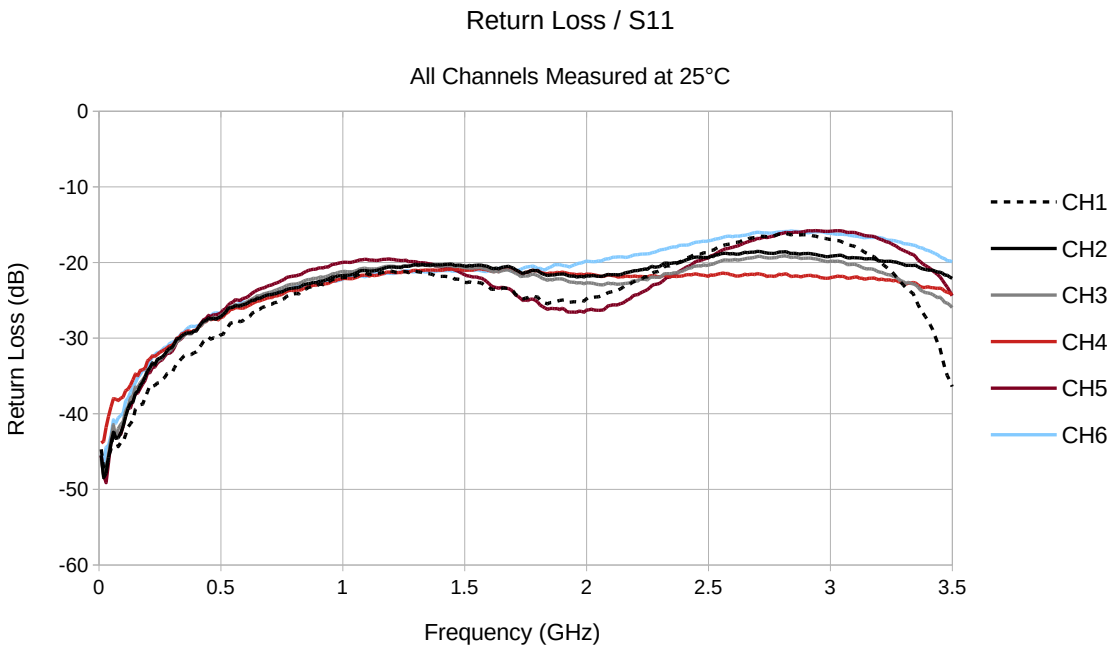


Figure 11. Typical Return Loss vs Frequency (S_{11})

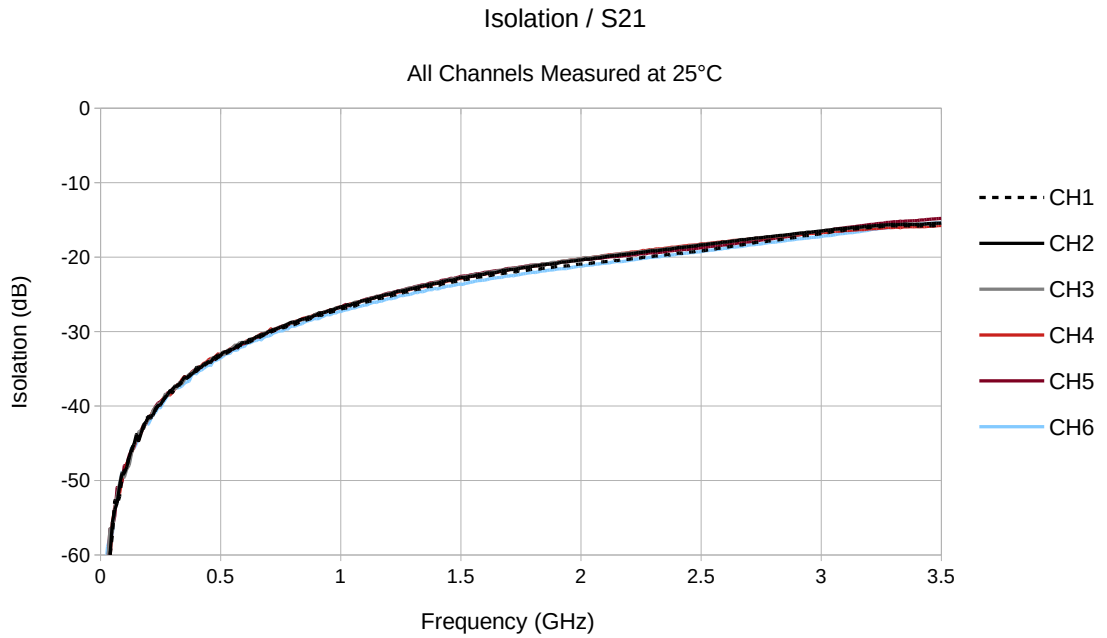


Figure 12. Typical Input to Output Isolation vs Frequency (S_{21} with Channel Off/Open)

Switching Reliability Test Results

Switch Hold-Down duration predictions and actuation cycling reliability test results are plotted below. Hold Down median failure is predicted to be >51500 days (>141 years) @ 50ºC and >1330 days (>3.6 years) @ 85ºC. Failure criteria is 20% change in pull in voltage and is based on creep model extrapolation of 1000 hours Hold Down test data.

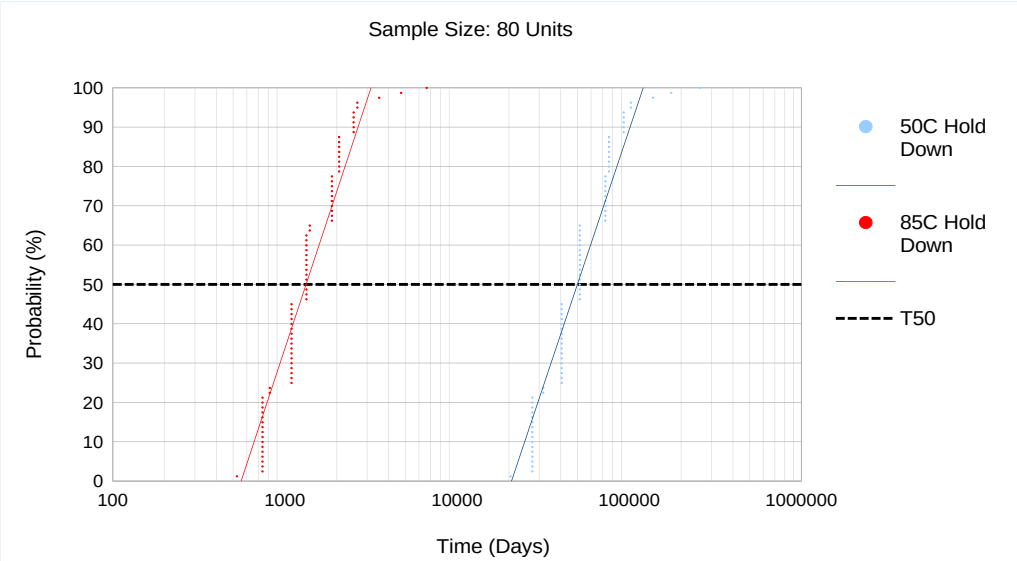


Figure 13. Hold Down: Days to Failure

Cycling median failure is greater than 30 billion cycles @ 25 ºC.

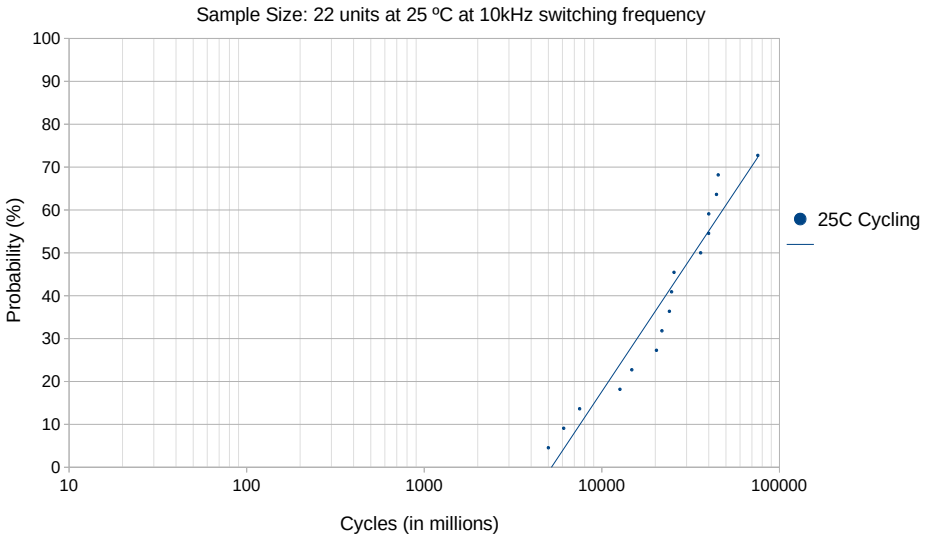


Figure 14. Cycling to Failure

Note: Failure is defined as stuck closed.

Hot switched actuation cycling reliability per channel test results are plotted below with voltage varied between 2 V and 5 V with a 71.5 Ω resistive load.

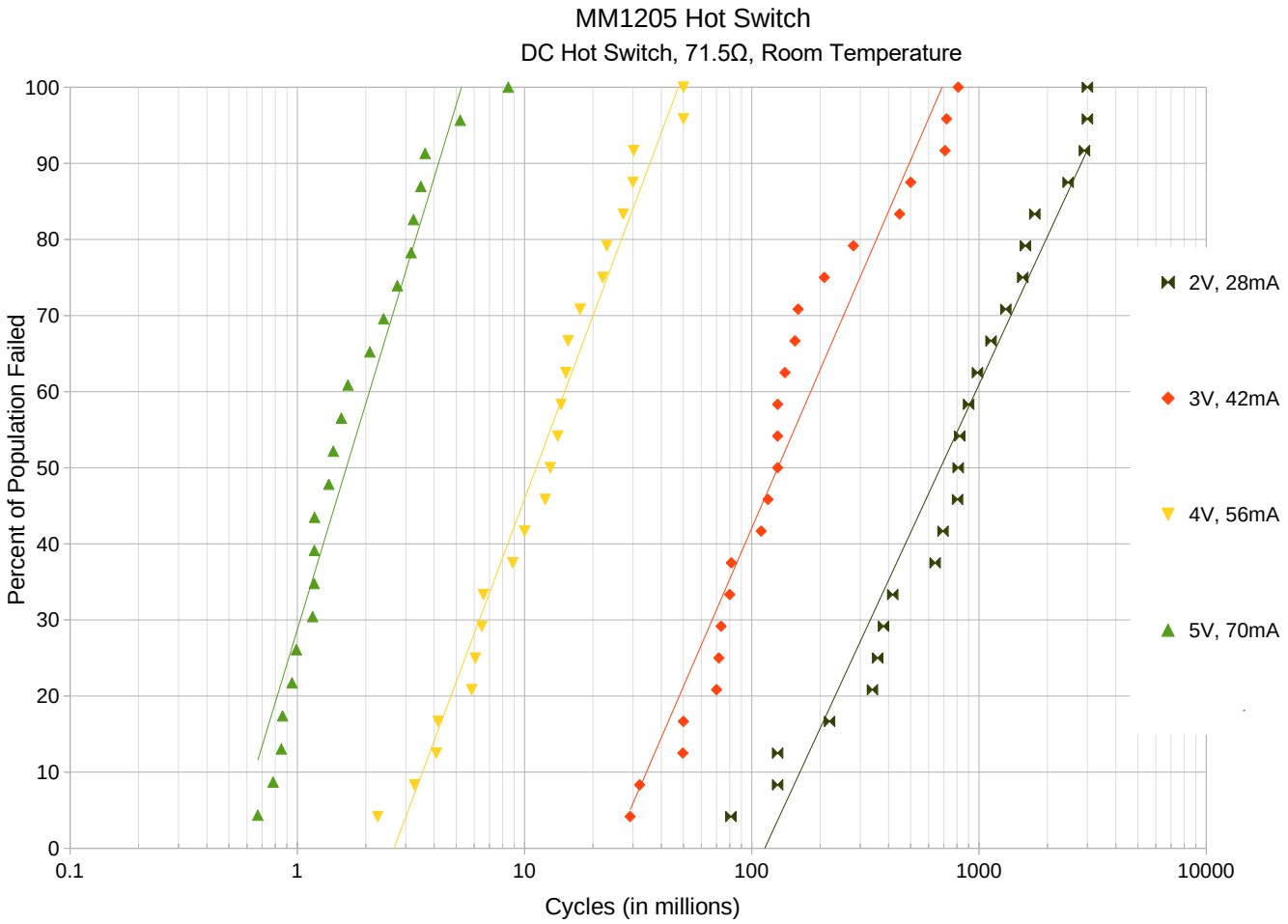


Figure 15. Hot Switch Endurance Test Results

Programming

Communication Interface

The MM1205 has two modes of operation; **SPI (serial)** and **GPIO (Parallel)**, selected by the **MODE** input pin.

All the SPI pins except the SSB pin and the MODE pin have an internal pull-down resistor to ensure that no digital input pins can float. The SSB pin has a pull-up current source in SPI mode. This ensures that the IC defaults to a disabled state in SPI mode. In GPIO mode, this pin is CTL4. In this case, the SSB pin has a pull-down resistor. This ensures that the input is low by default in GPIO mode.

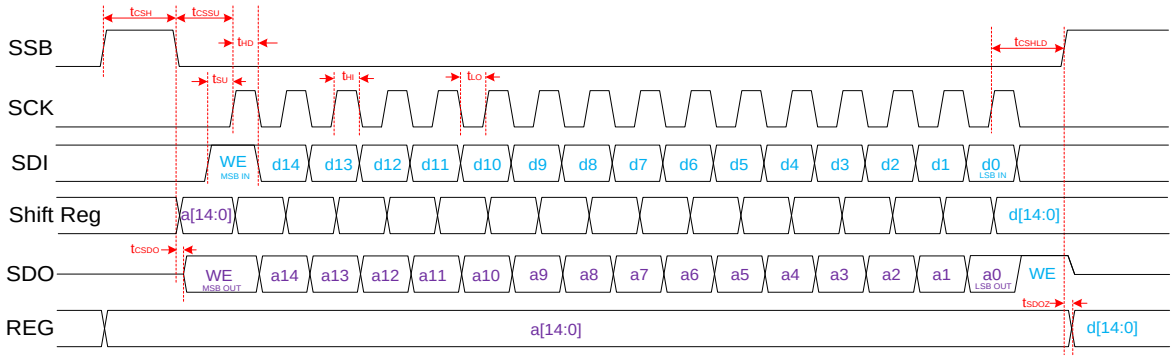


Figure 16. Timing Diagram

SPI Communication

MODE = 0, activates the 16-Bit Serial Peripheral Interface (SPI) module for operation. Multiple devices can be daisy-chained to drive multiple ICs using one SPI bus. (See Daisy Chain Operation, Figure 19 through Figure 21). The SPI works at any frequency up to a maximum of 33 MHz and may operate at significantly lower frequencies if the logic signals adhere to the data setup and hold requirements.

SPI Interface Mode

SPI timing diagrams are provided in Figure 16 through Figure 21. In SPI mode, data transmission starts when SSB goes Low, causing the Target to output the Most Significant Bit (MSB) of data to the SDO (MISO) pin. Data transfer from Host to Target takes place during the rising edge of the clock (SCK), which is idle when SSB is High. This mode of operation requires data for Host and Target to be present on SDI (MOSI) before the rising edge of the clock (defining SDI to SCK setup time). Data is pushed out of the SDO (MISO) pin during the falling edge of the clock. After the first 16-bit transaction, the Host writes the latest data (DN) to the Target, while the Target passes its previous (DN-1) stored data to the Host. Data is latched into the internal registers at the rising edge of SSB, if WR_EN = 1.

SPI Data Format

SPI data is sent in a 16-bit format. The first MSB bit (WE), if high, enables the Write mode. The following 7 MSB bits hold the Control and Fault Status bits. The 8 LSB bits hold the Switch State bits.

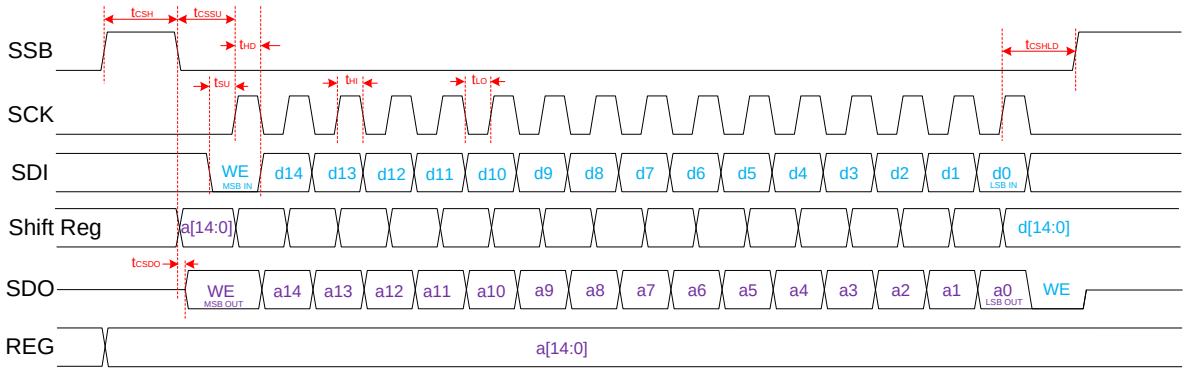


Figure 17. SPI Read Only (1 IC, No Daisy Chain)

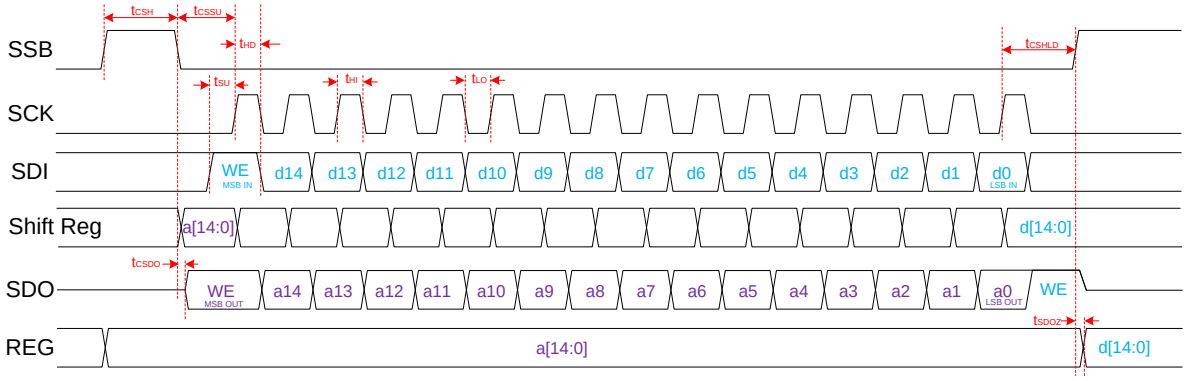


Figure 18. SPI Read & Write (1 IC, No Daisy Chain)

SPI Control Register

The SPI interface provides access to two 8-bit Internal Registers: Register STATE and Register CONTROL that are Read/Write registers. Register data is read by toggling SSB low and monitoring the data at the MISO pin while clocking the SCK pin. Register STATE holds the state of the 6 switches and is updated when SSB goes from LOW to HIGH, if the Write Enable bit is high. Register CONTROL holds four control bits (CPEN, V_{PPCOMP}, FLT_MODE, and SLEEP), and the fault status bit (FSTAT). The MSB bit enables the Write mode if high. In SPI mode, the CP_EN and FLT_MODE pins are ignored. Settings in the CONTROL register are used instead.

Note: The first row of the register tables below shows the read/write type, and default state. At power-on-reset (POR), all bits in both registers are set to LOW internally.

State Register

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
0	0	CTL6	CTL5	CTL4	CTL3	CTL2	CTL1
bit7							bit 0

bit 7: **Low**

Set this bit low

bit 6: **Low**

Set this bit low

bit 5: **CTL6**

1 = IN6 to OUT6 is Enabled

0 = IN6 to OUT6 is Disabled

bit 4: **CTL5**

1 = IN5 to OUT5 is Enabled

0 = IN5 to OUT5 is Disabled

bit 3: **CTL4**

1 = IN4 to OUT4 is Enabled

0 = IN4 to OUT4 is Disabled

bit 2: **CTL3**

1 = IN3 to OUT3 is Enabled

0 = IN3 to OUT3 is Disabled

bit 1: **CTL2**

1 = IN2 to OUT2 is Enabled

0 = IN2 to OUT2 is Disabled

bit 0: **CTL1**

1 = IN1 to OUT1 is Enabled

0 = IN1 to OUT1 is Disabled

Control Register

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
WR_EN	FSTAT	SLEEP	FLTMODE	V_{PPCOMP}	X	CPEN	X
bit7							bit 0

bit 7: **WR_EN**

1 = Enable write mode

0 = Disable Write mode (read only)

bit 6: **FSTAT**[1]

1 = V_{PP} OR V_{DD} Fault status = faulted

0 = V_{PP} OR V_{DD} Fault status = NOT faulted

bit 5: **SLEEP**

1 = SLEEP mode active (all analog circuits disabled)

0 = SLEEP mode inactive (all analog circuits enabled)

bit 4: **FLTMODE**

1 = Fault Mode Disabled (shutdown Disabled)

0 = Fault Mode Enabled (shutdown Enabled)

bit 3: **V_{PPCOMP}**

1 = V_{PP} under-voltage comparator is disabled

0 = V_{PP} under-voltage comparator is active

bit 2: **Do Not Care**

This bit can be set to either state without effecting performance.

bit 1: **CPEN**

1 = Charge Pump is enabled

0 = Charge Pump is disabled

bit 0: **Do Not Care**

This bit can be set to either state without effecting performance.

Note: After this bit is set high, it must be written to 0 to clear the fault. If fault mode is enabled, CPEN must be toggled to restart the charge pump. See Fault Conditions for more information.

Daisy Chain Operation

Daisy chaining the ICs is permitted and involves connecting the SDO (MISO) of one chip to the SDIN (MOSI) of the next chip in the chain, as shown in Figure 19. SPI timing diagrams with daisy-chained devices are provided in Figure 20 and Figure 21.

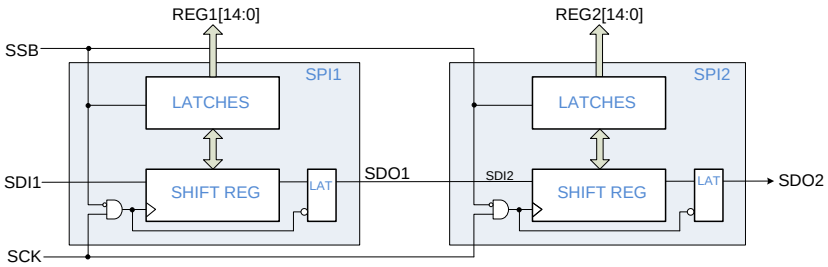


Figure 19. SPI with 2 ICs Daisy-chained

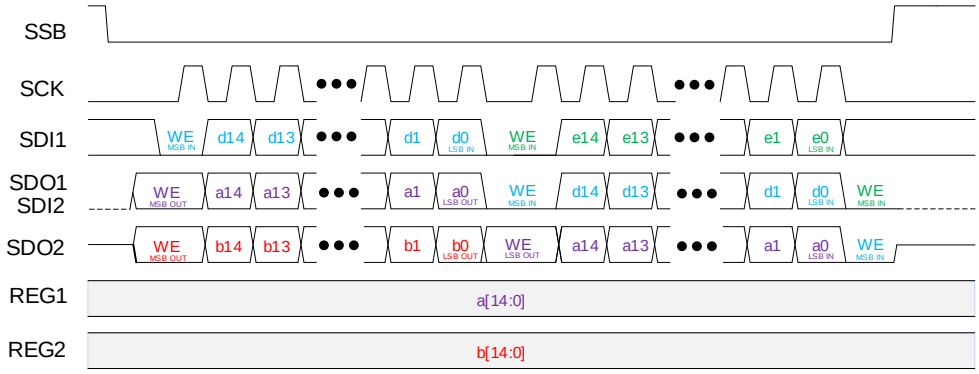


Figure 20. SPI Read Only (2 ICs Daisy-chained)

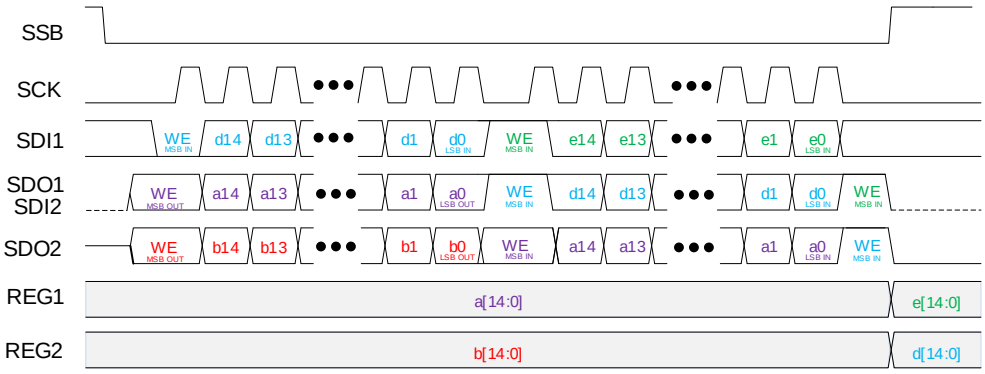


Figure 21. SPI Read & Write (2 ICs Daisy-chained)

GPIO Communication

MODE = 1 activates the GPIO (General Purpose Input Output or Parallel Mode) Communication Mode. In this mode of operation, the SPI Interface pins act as parallel inputs, as described in Table 8. Detailed Pin Description. Valid switch states are listed here.

Table 9. Switch State Table in GPIO Mode

#	FLIP_BIT	CTL4	CTL3	CTL2	CTL1	SW6	SW5	SW4	SW3	SW2	SW1
0	1	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF
1	1	0	0	0	1	OFF	OFF	OFF	OFF	OFF	**ON**
2	1	0	0	1	0	OFF	OFF	OFF	OFF	**ON**	OFF
3	1	0	0	1	1	OFF	OFF	OFF	**ON**	OFF	OFF
4	1	0	1	0	0	OFF	OFF	**ON**	OFF	OFF	OFF
5	1	0	1	0	1	OFF	**ON**	OFF	OFF	OFF	OFF
6	1	0	1	1	0	**ON**	OFF	OFF	OFF	OFF	OFF
7	1	0	1	1	1	OFF	OFF	OFF	OFF	OFF	OFF
8	1	1	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF
9	1	1	0	0	1	**ON**	OFF	**ON**	OFF	OFF	**ON**
10	1	1	0	1	0	**ON**	OFF	OFF	**ON**	**ON**	OFF
11	1	1	0	1	1	OFF	**ON**	**ON**	OFF	**ON**	OFF
12	1	1	1	0	0	**ON**	OFF	**ON**	OFF	**ON**	OFF
13	1	1	1	0	1	**ON**	OFF	**ON**	OFF	**ON**	OFF
14	1	1	1	1	0	OFF	**ON**	OFF	**ON**	OFF	**ON**
15	1	1	1	1	1	OFF	OFF	OFF	OFF	OFF	OFF
16	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF
17	0	0	0	0	1	OFF	OFF	OFF	OFF	OFF	**ON**
18	0	0	0	1	0	OFF	OFF	OFF	OFF	**ON**	OFF
19	0	0	0	1	1	OFF	OFF	OFF	OFF	**ON**	**ON**
20	0	0	1	0	0	**ON**	OFF	OFF	**ON**	OFF	OFF

#	FLIP_ BIT	CTL4	CTL3	CTL2	CTL1	SW6	SW5	SW4	SW3	SW2	SW1
21	0	0	1	0	1	**ON**	OFF	OFF	**ON**	OFF	**ON**
22	0	0	1	1	0	**ON**	OFF	OFF	**ON**	**ON**	OFF
23	0	0	1	1	1	**ON**	OFF	OFF	**ON**	**ON**	**ON**
24	0	1	0	0	0	OFF	**ON**	**ON**	OFF	OFF	OFF
25	0	1	0	0	1	OFF	**ON**	**ON**	OFF	OFF	**ON**
26	0	1	0	1	0	OFF	**ON**	**ON**	OFF	**ON**	OFF
27	0	1	0	1	1	OFF	**ON**	**ON**	OFF	**ON**	**ON**
28	0	1	1	0	0	**ON**	**ON**	**ON**	**ON**	OFF	OFF
29	0	1	1	0	1	**ON**	**ON**	**ON**	**ON**	OFF	**ON**
30	0	1	1	1	0	**ON**	**ON**	**ON**	**ON**	**ON**	OFF
31	0	1	1	1	1	**ON**	**ON**	**ON**	**ON**	**ON**	**ON**

Fault Conditions

There are two comparators that can signal a fault condition - V_{DD} under voltage fault and V_{PP} under voltage fault. Faults are reported differently depending on the mode of communication - SPI or GPIO.

Note: The V_{PP} under voltage comparator can be disabled. In SPI mode, it is disabled when the V_{PPCOMP} bit in the CONTROL register is high. In GPIO mode, the comparator is disabled when the CP_EN pin is set low.

The outputs of the V_{DD} and V_{PP} fault comparators are logically OR'ed. The output of the OR gate controls the FLTB pin. FLTB is an open-drain output and is ON (low impedance) if either fault is detected. In SPI mode, bit 6 of the CONTROL register provides V_{DD} and V_{PP} fault status.

At start-up, the FLTB pin is held OFF (high impedance). It is allowed to change state only after each voltage goes past its Enable threshold (V_{DD} goes higher than $UVLO_{RISE}$ and V_{PP} goes higher than V_{EN}). This prevents a race condition at startup.

Once V_{DD} and V_{PP} go above their thresholds, the comparators monitoring V_{DD} and V_{PP} actively monitor for faults. If V_{DD} goes below $UVLO_{FALL}$ or V_{PP} goes below V_{PPDIS}, a fault condition is signaled by setting the FLTB pin low and the Fault Status bit high (bit 6 in the CONTROL register). The FLTB pin returns to an open state when the fault condition is cleared and the FSTAT bit remains latched high until it is cleared via a SPI write. If Fault Mode is enabled (in GPIO mode, FLT_MODE pin = 0, in SPI mode, FLT_MODE bit = 0), the internal

high-voltage outputs are all set low (all switches open) and the charge pump is turned off. The user must toggle the CP_EN pin (GPIO mode) or the CPEN register bit (SPI mode) low and then high to restart the device.

If Fault Mode is disabled (in GPIO mode, FLT_MODE pin = 1; in SPI mode, FLT_MODE bit = 1), no action is taken by the IC. The fault condition is reported but does not affect the charge pump operation or switch states.

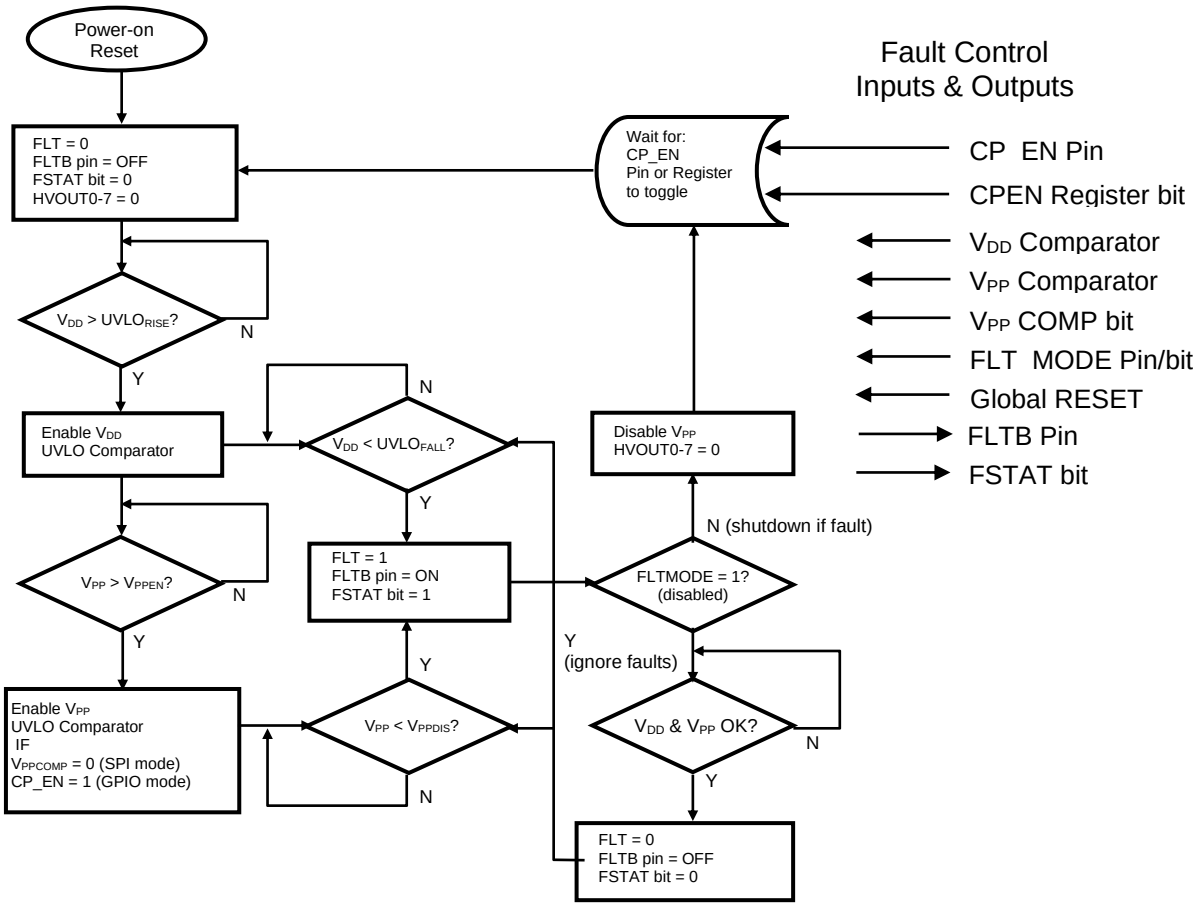


Figure 22. Flowchart for Fault

Notes:

1. The un-faulted supply continues to be monitored when a fault occurs. The FLT signal remains faulted until both supplies are above their brownout trip level.
2. V_{DD_IO} is not monitored unless it is connected to V_{DD}.
3. V_{PP} is not monitored if: V_{PPCOMP} = 1 in SPI mode or the CP_EN pin is low in GPIO mode.

Application Circuit Diagram

The MM1205 internal driver requires external circuitry to operate its charge pump. Figure 23 and Table 10 show the suggested bypass capacitors that have been used with good results. Menlo Micro recommends selecting components with equal or better performance.

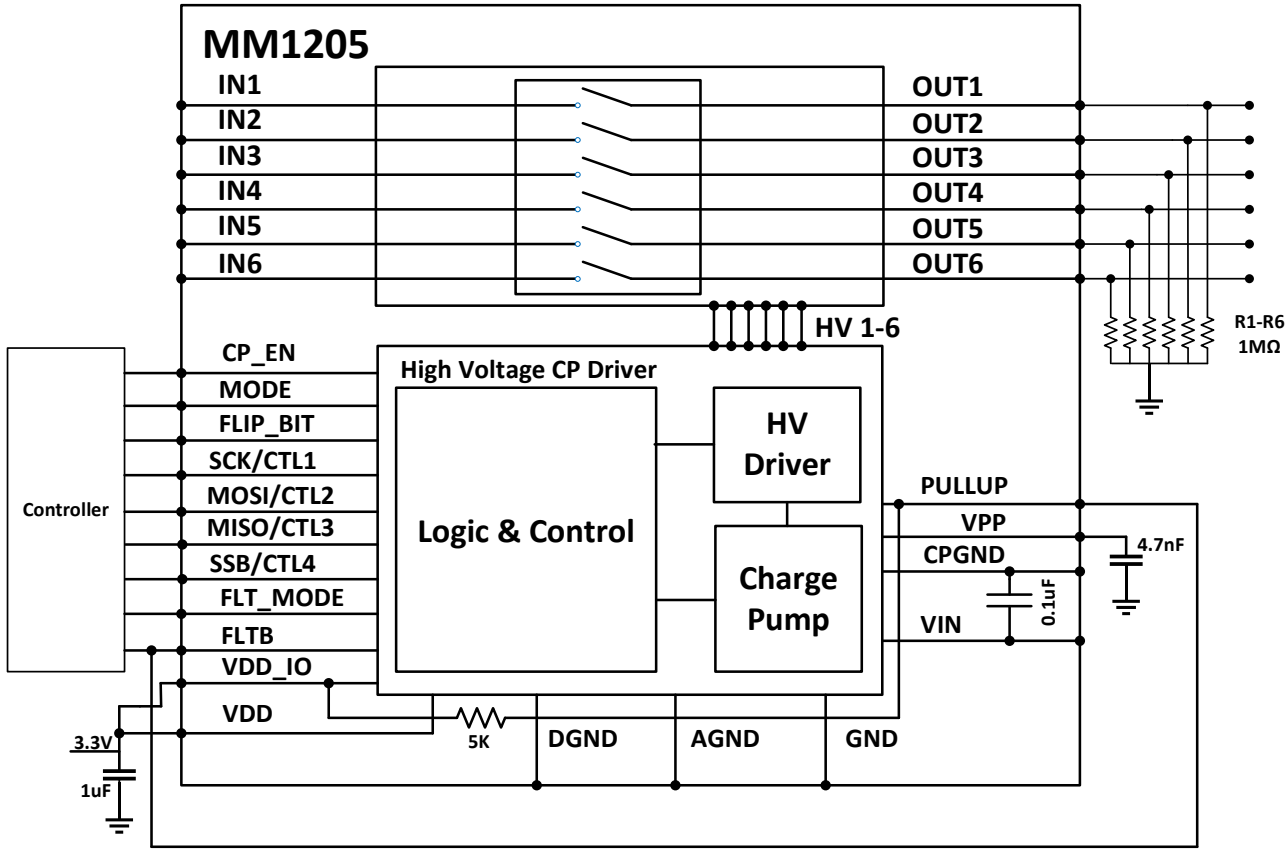


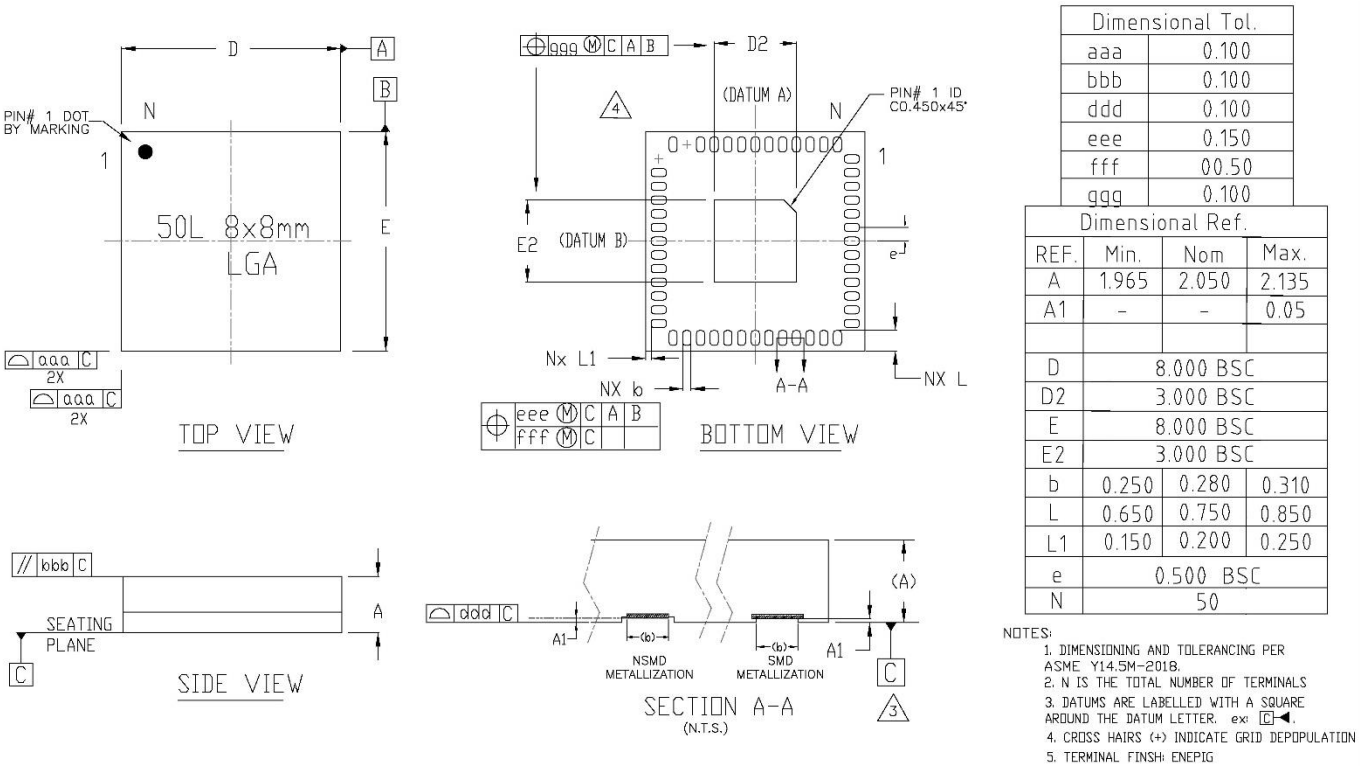
Figure 23. MM1205 Application Diagram

Table 10. Recommended Components for Application Circuit

Part Number	Value	Description
CHV0603N250472KXT	4.7nF	4700 pF ±10% 250V Ceramic Capacitor X7R 0603
C1608X5R1H105K080AB	1uF	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0603 50VDC 1uF 10% X5R 0.8mm
ERJ-2RKF1004X	1MΩ	RES 1M OHM 1% 1/10W 0402

Package Drawing

50 Lead LGA



Dimensional Tol.	
aaa	0.100
bbb	0.100
ddd	0.100
eee	0.150
fff	00.50
ggg	0.100

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.965	2.050	2.135
A1	-	-	0.05
D		8.000 BSC	
D2		3.000 BSC	
E		8.000 BSC	
E2		3.000 BSC	
b	0.250	0.280	0.310
L	0.650	0.750	0.850
L1	0.150	0.200	0.250
e		0.500 BSC	
N		50	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
2. N IS THE TOTAL NUMBER OF TERMINALS
3. DATUMS ARE LABELLED WITH A SQUARE AROUND THE DATUM LETTER. ex: C◀.
4. CROSS HAIRS (+) INDICATE GRID DEPOPULATION
5. TERMINAL FINSH: ENEPIG

Figure 24. Package Drawing

Recommended PCB Layout and SMT Parameters

- PCB pad pattern diagram is shown in Figure 25.
- Connect exposed pad in the center of package to Signal Ground.
- Type 3 or higher solder paste.
- Component placement force not to exceed 100 grams.
- For best performance, maximize solder coverage of the thermal pad.

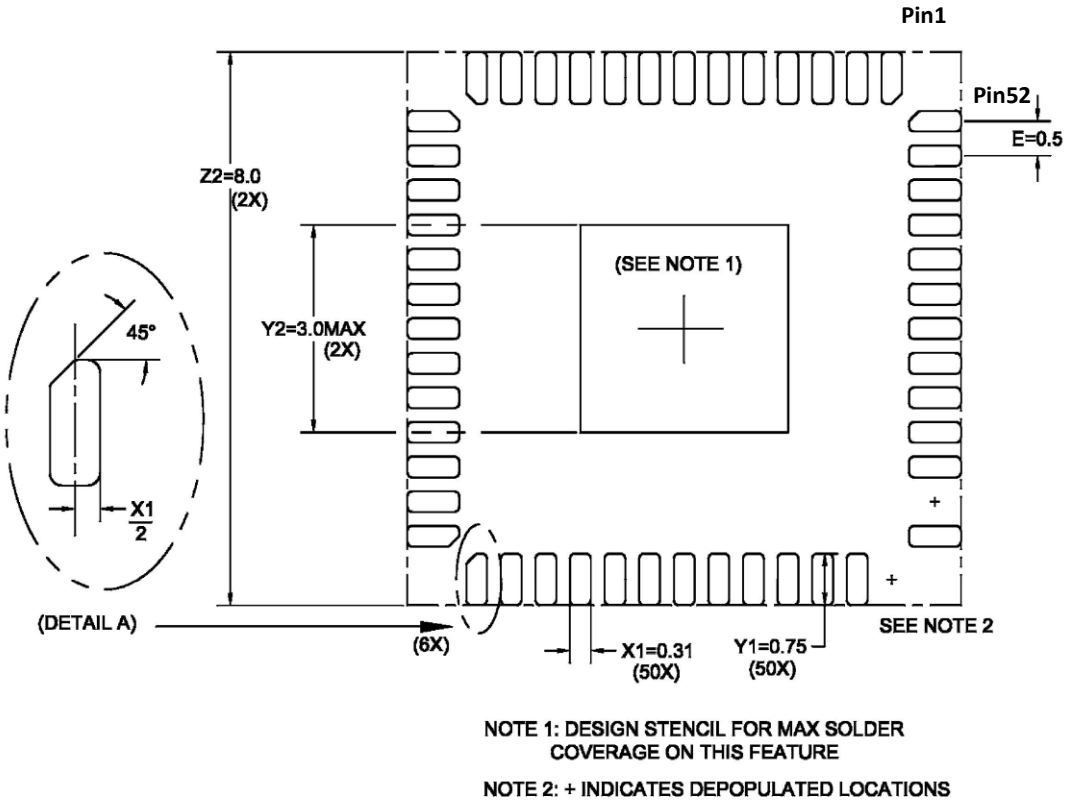


Figure 25. Recommended PCB Pad Pattern Top View

Recommended Solder Reflow Profile

This product has been qualified to a Moisture Sensitivity Level (MSL) 3 using a Pb-free reflow profile as specified in IPC/JEDEC-Std-20e (ref: tables 4.2, 5.2, and Figure 5.1).

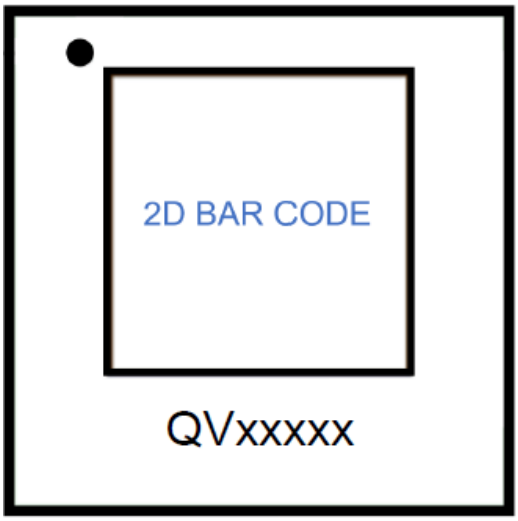
SMT reflow of this product to a PCB should not exceed the temperature profile stated in this specification.

Storage and Shelf Life

Under typical industry storage conditions (≤30 °C/60% RH) in Moisture Barrier Bags the following is recommended:

- Customer Shelf Life: 24 months from customer receipt date
- Extended Shelf Life: 60 months from customer receipt date if re-bagged every 24 months or less

Package Marking Information



Dot ● = Pin 1 Indicator
Line 1 = 2D Bar Code
Line 2 = Human-readable product code

Figure 26. Package Marking Drawing

Package Materials Information

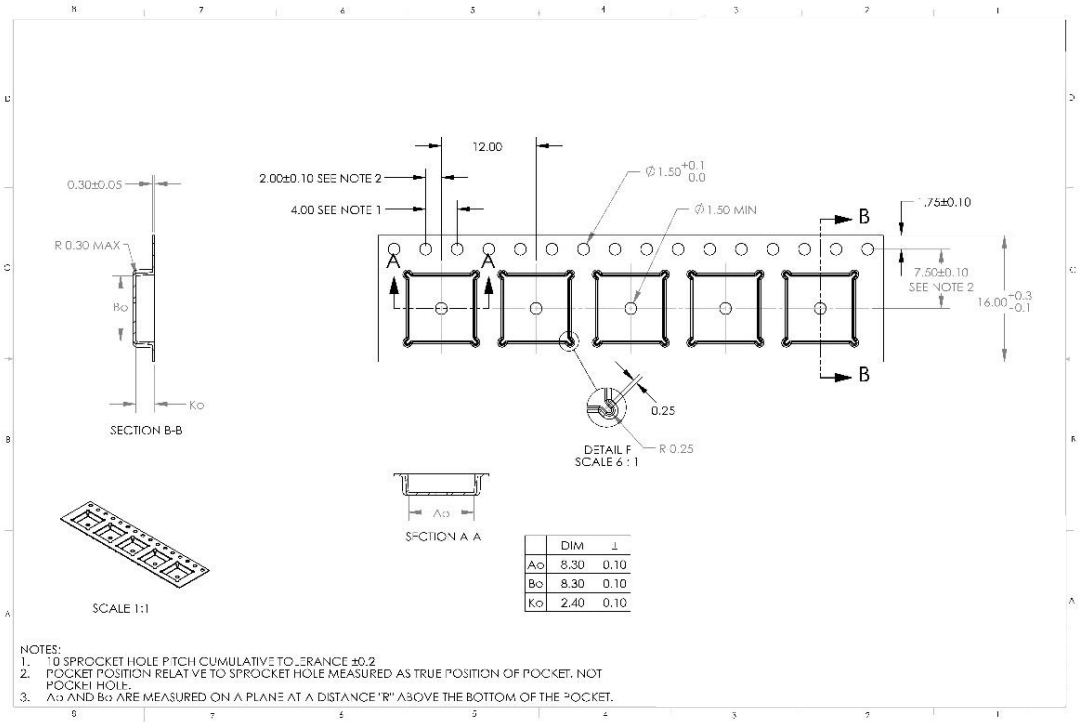


Figure 27. Tape and Reel Drawing

Package Options and Ordering Information

All Menlo Micro solutions are EAR99 compliant.

Part Number	Package	Temperature Range	Device Marking[1]
MM1205-01NDB	30V/1A, DC-3GHz - 6xSPST - w/internal charge pump - 8mm x 8mm LGA Industrial Temp	-40°C to +85°C	QVxxxxx
MM1205-01NDB-TR	30V/1A, DC-3GHz - 6xSPST - w/internal charge pump - 8mm x 8mm LGA Industrial Temp, Tape and Reel (Qty 250)[2]	-40°C to +85°C	QVxxxxx
MM1205EVK1	Evaluation board for MM1205, 30V/1A - 6xSPST w/internal charge pump - 8mm x 8mm LGA		
MM1205EVK2	Evaluation board for MM1205, DC-3GHz - 6xSPST w/internal charge pump - 8mm x 8mm LGA		

Notes:

1. Additional markings may be present, including logo or lot trace code information. This information may be a 2D barcode or other human-readable markings. Note that 'x' is a placeholder for a 5-digit numerical code.
2. 250pcs standard tape and reel increment

Important Information

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For product technical questions and application information: support@menlomicro.com.

