Hiteca™

"Hiteca™" Range of low loss, high stability Class II Capacitors

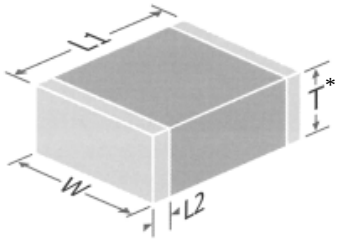
Hiteca™ Range of Ceramic Capacitors

The Hiteca™ range of MLCCs utilises a unique patented dielectric system that offers improved capacitance stability and lower parasitic losses under common operating conditions, compared to standard Class II dielectrics such as X7R.

Combined with a capacitance ageing rate of 0, this range is particularly suited for applications such as DC bus and snubber capacitors, where high capacitance values under full rated voltage are required.

The inherent low loss enables these devices to handle much higher ripple currents that conventional ceramic capacitors, making them market leaders for power electronic applications.

Electrical Details	
Capacitance Range	See website for latest range
Temperature Coefficient of Capacitance (TCC)	±15% max (typically +0% to -10%)
Typical capacitance drop at maximum operating voltage	<45%
Insulation Resistance (IR)	100GΩ or 1000secs (whichever is the less)
Dielectric Withstand Voltage (DWV)	Voltage applied for 5seconds max, 50mA charging current maximum
Ageing Rate	Zero
Operating Temperature Range	-55ºC / +125ºC



Size	Length L1** in mm (inches)	Width W in mm (inches)	Band L2 in mm (inches)
1206	3.2 +0.30/-0.20 (0.126 +0.012/-0.008)	1.6 ± 0.20 (0.063 ± 0.008)	0.25 – 0.75 (0.010 - 0.030)
1210†	3.2 +0.30/-0.20 (0.126 +0.012/-0.008)	2.5 ± 0.20 (0.098 ± 0.008)	0.25 – 0.75 (0.010 - 0.030)
1812	4.5 +0.40/-0.30 (0.180 +0.016/-0.012)	3.2 ± 0.2 (0.126 ± 0.00)	0.25 – 1.143 (0.010 - 0.045)
1825	4.5 +0.40/-0.30 (0.180 +0.016/-0.012)	6.4 ± 0.4 (0.252 ± 0.016)	0.25 – 1.0 (0.010 - 0.040)
2220	5.7 +0.50/-0.40 (0.225 +0.02/-0.016)	5.0 ± 0.4 (0.197 ± 0.016)	0.25 – 1.0 (0.010 - 0.040)
2225	5.7 +0.50/-0.40 (0.225 +0.02/-0.016)	6.3 ± 0.4 (0.252 ± 0.016)	0.25 – 1.143 (0.010 - 0.045)

** For thickness (T) measurements, refer to min-max capacitance value tables on the following page*
*** Length (L1) data shown is for FlexiCap™ termination (termination code Y). For unplated solderable silver termination (termination code 8), subtract 0.1mm (0.004") from maximum length. For example, length of 1206 with 8 termination is 3.2 ±0.20mm (0.126 ± 0.008")*
† 1210 Length (L1) and width (W) dimensions are for standard thickness parts. For non-standard thickness parts, L1 = 3.2 +0.50/-0.20 (0.126 +0.020/-0.008) & W = 2.5 +0.40/-0.20 (0.098 +0.016/-0.008).

Ordering Information

4040	Y	500	0155	M	Z	B
Chip Size	**Termination**	**Voltage d.c.**	**Capacitance in Picofarads (pF)**	**Capacitance Tolerance**	**Dielectric**	**Packaging**
1206 **1210** **1812** **1825** **2220** **2225**	**Y** = FlexiCap™ polymer termination base with Ni barrier (100% matte tin plating, RoHS compliant) **8** = Unplated solderable silver (Z dielectric only, RoHS compliant)	**200** = 200V **250** = 250V **450** = 450V **500** = 500V **630** = 630V **700** = 700V **900** = 900V **1K0** = 1000V **1K2** = 1200V **1K5** = 1500V **2K0** = 2000V	First digit is 0. Second and third digits are significant figures of capacitance code. The fourth digit is the number of zeros following. e.g., **0101** = 100 pF Values are E24 series	**J**: ± 5% **K**: ± 10% **M**: ± 20%	**Z =** Hiteca™ low loss stable (Standard Commercial) **Y =** Hiteca™ low loss stable (AEC-Q200)	**T** = 178mm (7") reel **R** = 330mm (13") reel **B** = Bulk pack – tubs or trays

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Minimum/Maximum Capacitance Values

Note: Knowles Precision Devices operate a continuous improvement process with ranges being expanded and updated regularly. The latest range may differ. Please contact the local sales office or refer to the KPD website – www.knowlescapacitors.com

These values are guidelines only. Please contact your local sales office to discuss your specific requirements.

Standard thickness parts (Standard Commercial & AEC-Q200 ranges):

Chip Size	1206	1210	1812	1825	2220	2225
Thickness T in mm (inches)	1.7 max (0.068 max)	2.0 max (0.08 max)	2.5 max (0.1 max)	2.5 max (0.1 max)	2.5 max (0.1 max)	2.5 max (0.1 max)
200Vdc	100pF - 33nF	100pF - 82nF	100pF - 220nF	220pF - 390nF	220pF - 390nF	470pF - 470nF
250Vdc	100pF - 33nF	100pF - 82nF	100pF - 220nF	220pF - 390nF	220pF - 390nF	470pF - 470nF
450Vdc	100pF - 18nF	100pF - 47nF	100pF - 150nF	220pF - 270nF	220pF - 270nF	470pF - 330nF
500Vdc	100pF - 15nF	100pF - 39nF	100pF - 120nF	220pF - 220nF	220pF - 220nF	470pF - 270nF
630Vdc	100pF - 10nF	100pF - 22nF	100pF - 68nF	220pF - 150nF	220pF - 150nF	470pF - 180nF
1000Vdc	100pF – 3.9nF	100pF - 10nF	100pF - 27nF	220pF - 56nF	220pF - 56nF	470pF - 68nF
1200Vdc	100pF – 2.7nF	100pF – 6.8nF	100pF - 18nF	220pF - 39nF	220pF - 39nF	470pF - 47nF
1500Vdc	100pF – 2.2nF	100pF – 4.7nF	100pF - 12nF	220pF - 22nF	220pF - 22nF	470pF - 33nF
2000Vdc	100pF - 1nF	100pF – 2.2nF	100pF – 6.8nF	220pF - 12nF	220pF - 12nF	470pF - 18nF

Non-standard thickness parts (Standard Commercial Range only):

Chip Size	1206	1210	1812	1825	2220	2225
Thickness T in mm (inches)	-	2.8 max (0.110 max)	3.2mm max (0.126 max)	4.0mm max (0.157 max)	4.0mm max (0.157 max)	4.0mm max (0.157 max)
200Vdc	-	100nF – 120nF	270nF – 270nF	470nF – 560nF	470nF – 560nF	560nF – 680nF
250Vdc	-	100nF – 120nF	270nF – 270nF	470nF – 560nF	470nF – 560nF	560nF – 680nF
450Vdc	-	56nF – 82nF	180nF – 180nF	330nF – 470nF	330nF – 470nF	390nF – 560nF
500Vdc	-	47nF - 56nF	150nF - 150nF	270nF - 390nF	270nF - 390nF	330nF - 470nF
630Vdc	-	27nF - 39nF	82nF - 100nF	180nF - 270nF	180nF - 270nF	220nF – 330nF
700Vdc	-	12nF – 33nF	33nF – 82nF	68nF – 220nF	68nF – 220nF	82nF – 270nF
900Vdc	-	12nF – 22nF	33nF – 47nF	68nF – 120nF	68nF – 120nF	82nF – 180nF
1000Vdc	-	12nF – 18nF	33nF - 39nF	68nF - 100nF	68nF - 100nF	82nF - 120nF
1200Vdc	-	8.2nF – 12nF	22nF – 27nF	47nF – 68nF	47nF – 68nF	56nF – 82nF
1500Vdc	-	5.6nF – 6.8nF	15nF – 18nF	27nF – 47nF	27nF – 47nF	39nF – 56nF
2000Vdc	-	2.7nF – 3.9nF	8.2nF – 10nF	15nF – 27nF	15nF – 27nF	22nF – 33nF

Some parts in this range may be subject to export controls. Refer to the section 'Export Controls and Dual-use Regulations' for full details.

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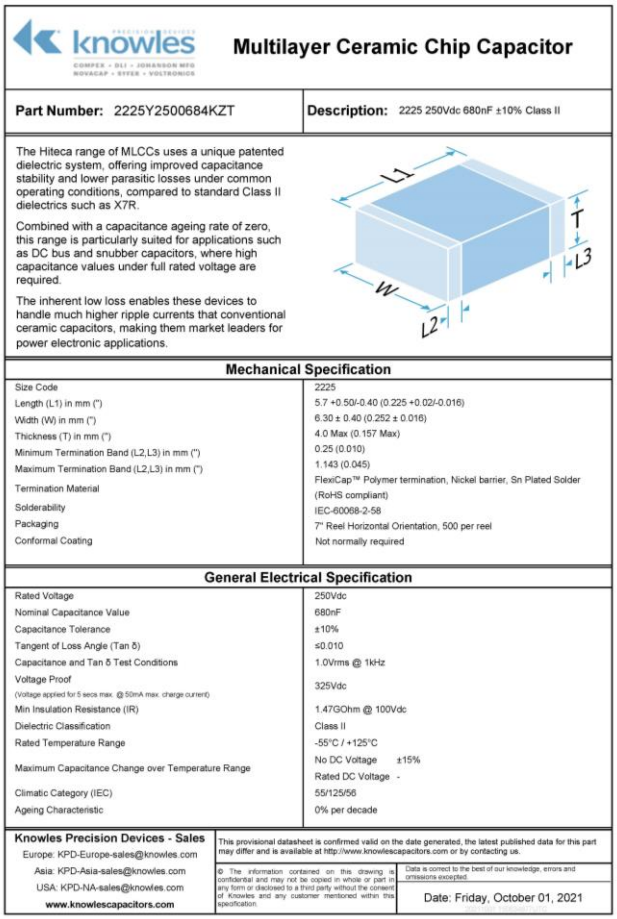
Datasheets and Environmental Certificates

Detailed individual datasheets and part specific environmental certificates can now be downloaded direct from the Knowles website (www.knowlescapacitors.com):



knowles

Multilayer Ceramic Chip Capacitor

Part Number: 2225Y2500684KZT **Description:** 2225 250Vdc 680nF ±10% Class II

The Hiteca range of MLCCs uses a unique patented dielectric system, offering improved capacitance stability and lower parasitic losses under common operating conditions, compared to standard Class II dielectrics such as X7R.

Combined with a capacitance ageing rate of zero, this range is particularly suited for applications such as DC bus and snubber capacitors, where high capacitance values under full rated voltage are required.

The inherent low loss enables these devices to handle much higher ripple currents that conventional ceramic capacitors, making them market leaders for power electronic applications.

Mechanical Specification

Size Code	2225
Length (L1) in mm (")	5.7 +0.50/-0.40 (0.225 +0.02/-0.016)
Width (W) in mm (")	6.30 ± 0.40 (0.252 ± 0.016)
Thickness (T) in mm (")	4.0 Max (0.157 Max)
Minimum Termination Band (L2,L3) in mm (")	0.25 (0.010)
Maximum Termination Band (L2,L3) in mm (")	1.143 (0.045)
Termination Material	FlexiCap™ Polymer termination, Nickel barrier, Sn Plated Solder (RoHS compliant)
Solderability	IEC-60068-2-58
Packaging	7" Reel Horizontal Orientation, 500 per reel
Conformal Coating	Not normally required

General Electrical Specification

Rated Voltage	250Vdc
Nominal Capacitance Value	680nF
Capacitance Tolerance	±10%
Tangent of Loss Angle (Tan δ)	≤0.010
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1kHz
Voltage Proof (Voltage applied for 5 secs max. @ 50mA max. charge current)	325Vdc
Min Insulation Resistance (IR)	1.47GOhm @ 100Vdc
Dielectric Classification	Class II
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage ±15% Rated DC Voltage -
Climatic Category (IEC)	55/125/56
Ageing Characteristic	0% per decade

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This provisional datasheet is confirmed valid on the date generated, the latest published data for this part may differ and is available at http://www.knowlescapacitors.com or by contacting us.

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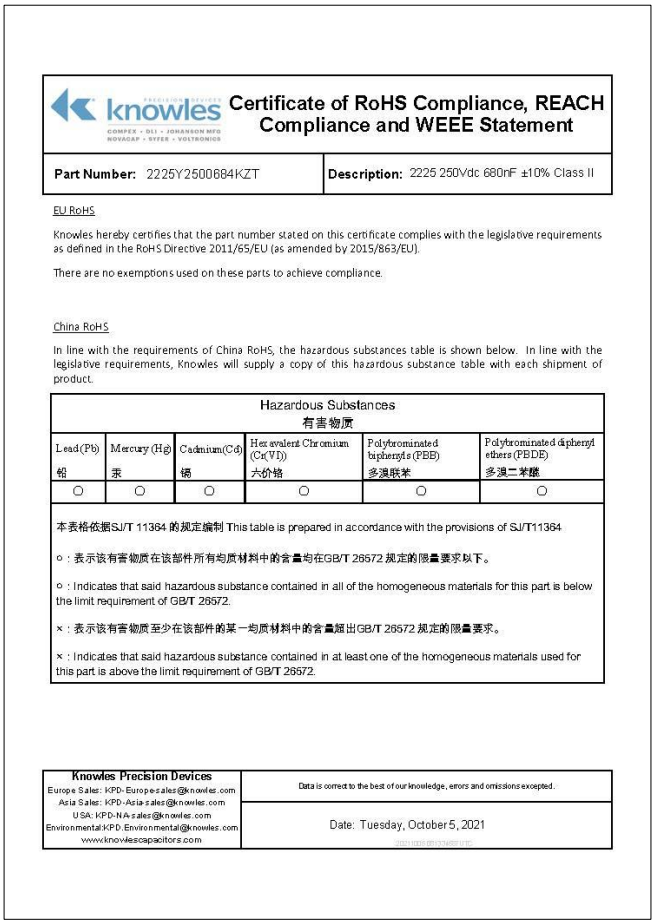
Data is correct to the best of our knowledge, errors and omissions excepted.

Date: Friday, October 01, 2021



knowles

Certificate of RoHS Compliance, REACH Compliance and WEEE Statement

Part Number: 2225Y2500684KZT **Description:** 2225 250Vdc 680nF ±10% Class II

EU RoHS

Knowles hereby certifies that the part number stated on this certificate complies with the legislative requirements as defined in the RoHS Directive 2011/65/EU (as amended by 2015/863/EU).

There are no exemptions used on these parts to achieve compliance.

China RoHS

In line with the requirements of China RoHS, the hazardous substances table is shown below. In line with the legislative requirements, Knowles will supply a copy of this hazardous substance table with each shipment of product.

Hazardous Substances
有害物质

Lead (Pb) 铅	Mercury (Hg) 汞	Cadmium (Cd) 镉	Hexavalent Chromium (Cr(VI)) 六价铬	Polybrominated biphenyls (PBB) 多溴联苯	Polybrominated diphenyl ethers (PBDE) 多溴二苯醚
○	○	○	○	○	○

本表格依据SJ/T 11364 的规定编制 This table is prepared in accordance with the provisions of SJ/T11364.

○：表示该有害物质在该部件所有均质材料中的含量均在GB/T 26572 规定的限量要求以下。

○ : Indicates that said hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement of GB/T 26572.

×：表示该有害物质至少在该部件的某一均质材料中的含量超出GB/T 26572 规定的限量要求。

× : Indicates that said hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement of GB/T 26572.

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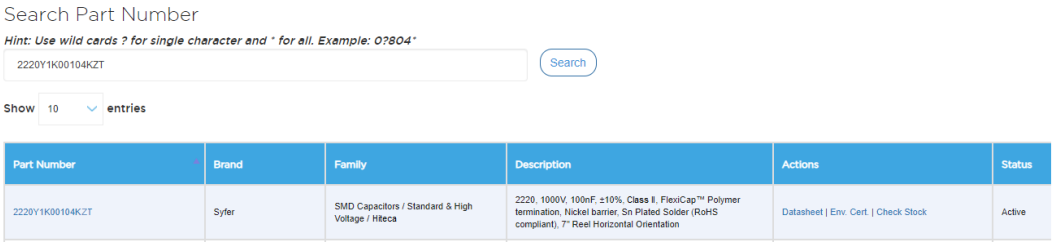
Data is correct to the best of our knowledge, errors and omissions excepted.

Date: Tuesday, October 5, 2021

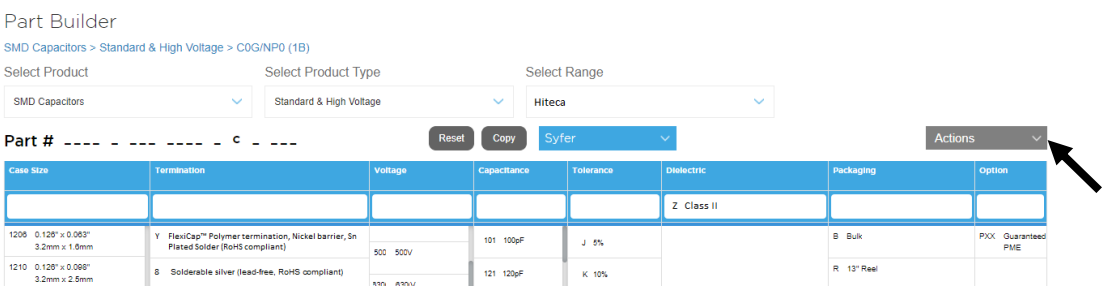
Knowles Precision Devices Sales contact e-mail	Europe:	KPD-Europe-sales@knowles.com
	Asia:	KPD-Asia-sales@knowles.com
	USA:	KPD-NA-sales@knowles.com

To generate the datasheet or environmental certificate for a part:

- If you know the part number, use the **MLC Part Search** application to search for the part, then choose Datasheet or Environmental Certificate in the Actions column:



- If you don't know the part number, use the **MLC Part Builder** application to specify the required properties (case size, termination, rated voltage, capacitance value, etc.), then click the Actions button (arrowed below) to generate the Datasheet or Environmental Certificate:

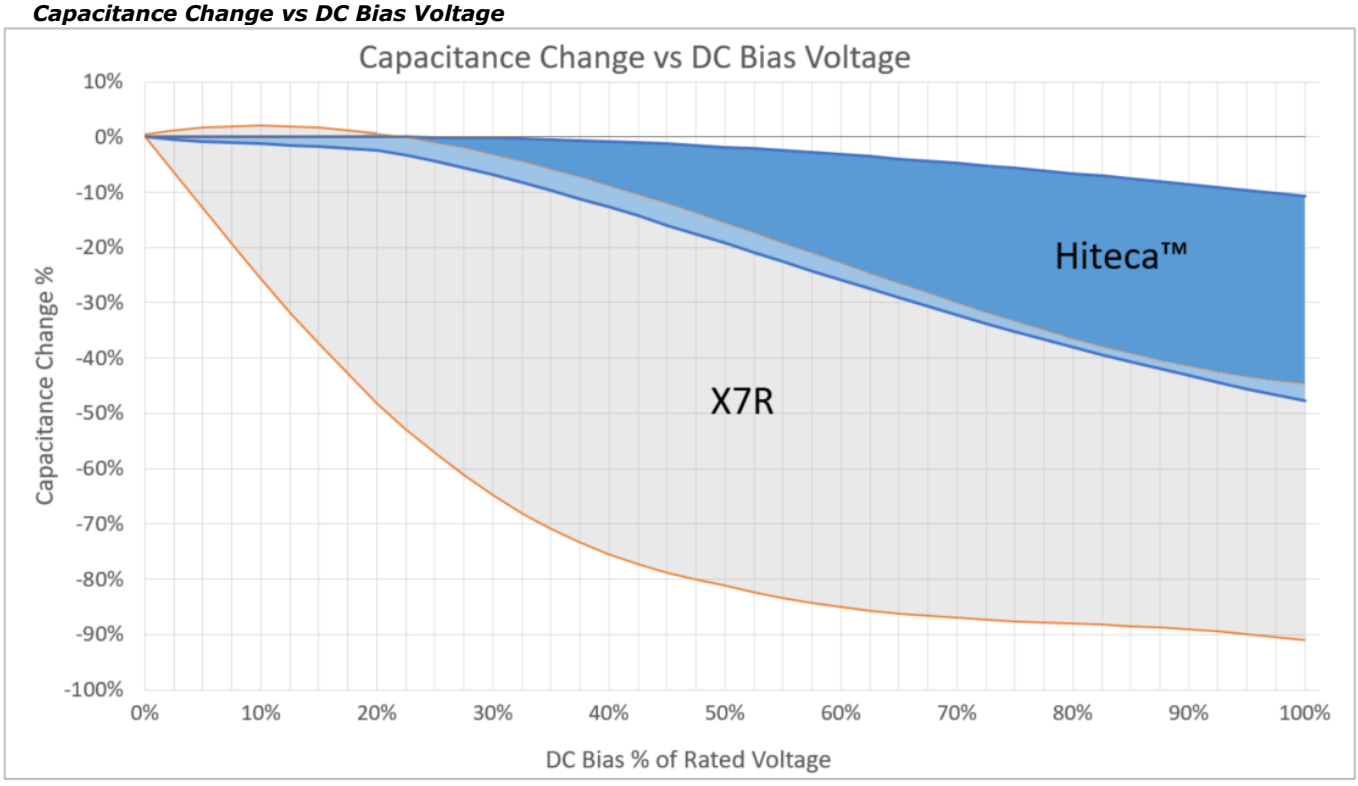


Typical Performance Curves

The following graphs show typical electrical characteristics for a range of sample Hiteca™ parts. They are representative only, and variations may occur between batches. This data does not constitute a specification.

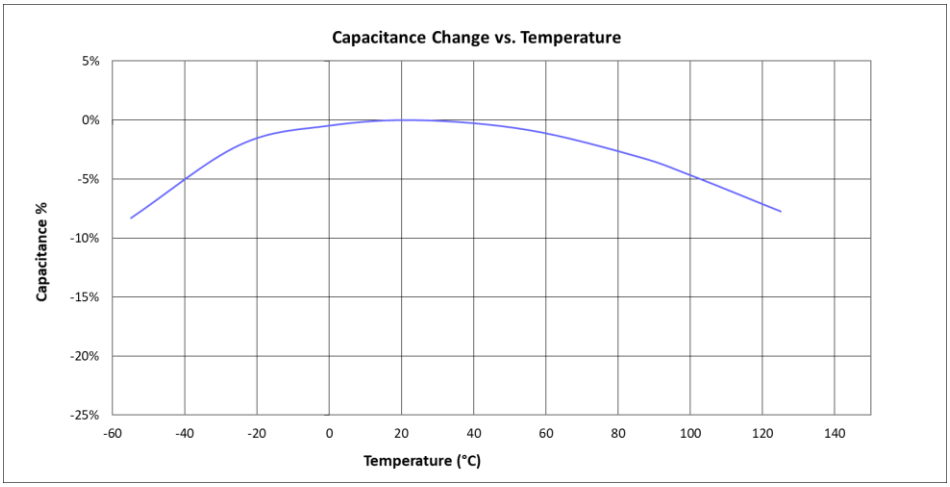
Impedance vs Frequency

Capacitance Change vs DC Bias Voltage



** Capacitance change for any Hiteca™ capacitor should lie within the blue shaded band, shown in comparison to values for X7R dielectric.*

Capacitance Change vs DC Temperature

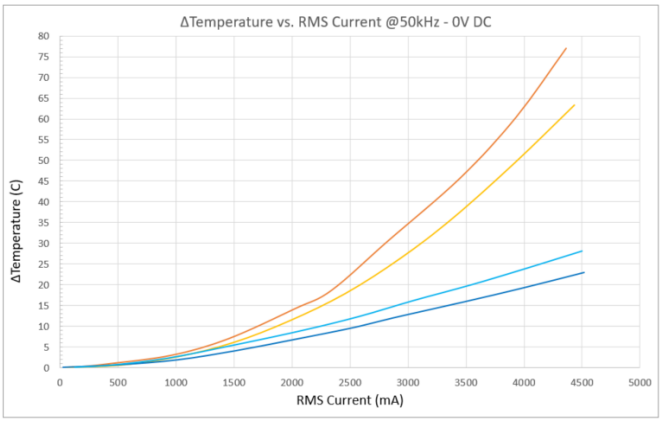


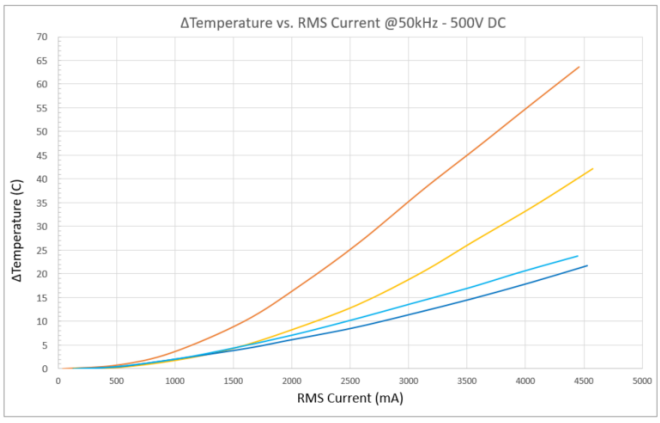
Temperature Rise vs Ripple Current

Comparison of Hiteca™, standard X7R and competitor X7T capacitors at different frequencies and DC bias voltages:

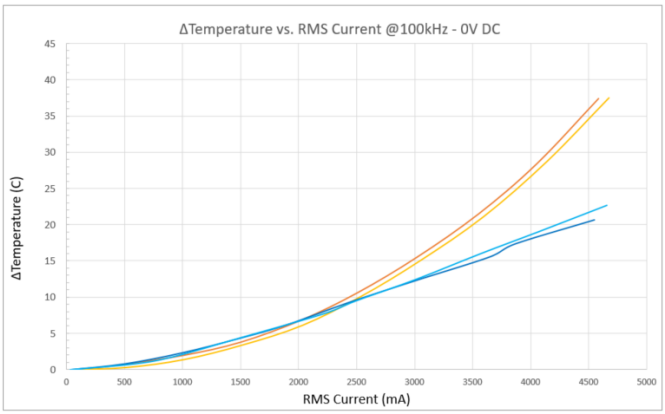
0V DC Bias | *500V DC Bias*

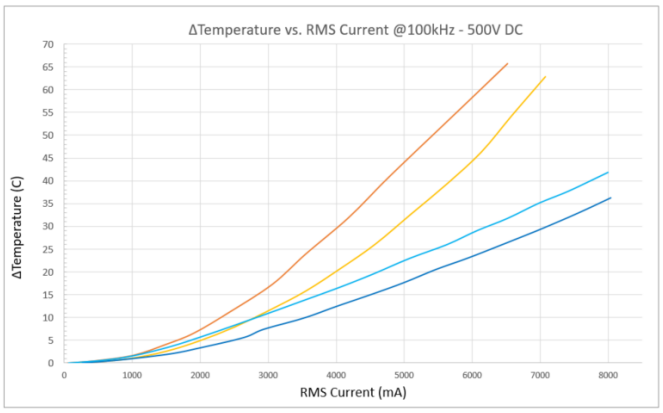
50kHz



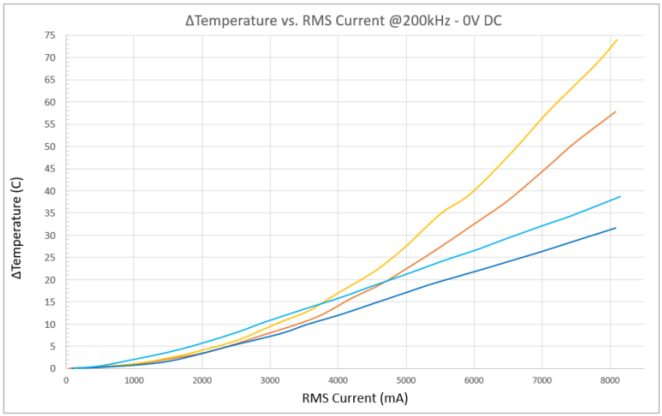


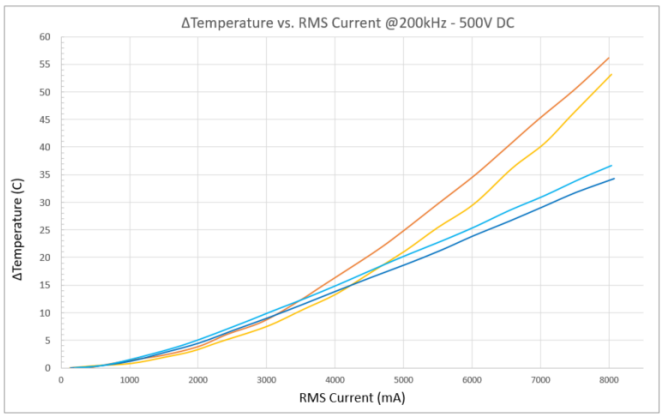
100kHz





200kHz





X7R 2220 1uF 630V — Competitor X7T 2220 1uF 630V — Hiteca™ 2220 390nF 500V — Hiteca™ 2225 330nF 630V

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Performance

Lot by lot inspection (all batches)

Test	Additional Requirements	Sample Size	Accept/Fail	Test Method	
Visual inspection	Inspect construction and workmanship	125	0/1	MIL-STD-883 Method 2009	10x magnification. Free of visual defects
Dimensions	Verify physical dimensions comply with specification	13	0/1	JESD22 Method JB-100	Digital Vernier or micrometer as applicable. Within specified tolerance
Capacitance	Class II 1kHz @ 1.0V	100%	N/a	CECC 32 100 Clause 4.6.1	Within specified tolerance
D.F.	Class II 1kHz @ 1.0V	100%	N/a	CECC 32 100 Clause 4.6.2	<0.01 @ 1kHz (Q > 100 @ 1kHz)
Voltage Proof / DWV	$V_R \leq 900V$: $V_P = 1.3 \times V_R$ $V_R \geq 1000V$: $V_P = 1.2 \times V_R$ Where: V_R = rated voltage, V_P = voltage proof test voltage	100%	N/a	CECC 32 100 Clause 4.6.4	No breakdown or flashover. R≥ 100MΩ or 1s, whichever is the smaller
I.R.	Test Voltage = 100V	100%	N/a	CECC 32 100 Clause 4.6.3	100GΩ or 1000secs (whichever is the less)
D.P.A.	-	29	0/1	EIA-469	Cut in both directions. Inspect and measure as applicable. Free from internal defects
Solderability	-	10	0/1	IEC 60068-2-58	Method 2: Reflow >95% coverage of critical area
Resistance to Soldering Heat	-	10	0/1	IEC 60068-2-58	Method 2: Reflow >95% coverage of critical area
Temperature Characteristic of Capacitance	Carried out for each manufacturing batch of dielectric material	-	-	CECC 32 100 Clause 4.7.2	Maximum TC ± 15% (typically +0% to -10%) over -55°C / +125°C, no DC voltage applied

Soldering Information

Reflow Soldering

Knowles recommends reflow soldering as the preferred method for mounting MLCCs. Hiteca™ MLCCs can be reflow soldered using the internationally recognised reflow profile defined in IPC/FEDEC J-STD-020. Flexicap™ ('Y') and unplated solderable silver ('8') terminations are compatible with both conventional and lead free soldering with peak temperatures of 260ºC to 270ºC being acceptable.

The heating ramp rate should be such that components see a temperature rise of 1.5ºC to 4ºC per second to maintain temperature uniformity through the MLCC.

The time for which the solder is molten should be maintained at a minimum, so as to prevent solder leaching.

For Flexicap™ ('Y') termination, extended times above 230˚C can cause problems with oxidation of Sn plating. Use of an inert atmosphere can help if this problem is encountered.

For unplated solderable silver ('8') termination, extended exposure to liquid solders can result in solder leach. Use of an inert atmosphere can be advantageous.

Cooling to ambient temperature should be allowed to occur naturally, particularly if larger chip sizes are being soldered. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced cooling should be avoided as this can induce thermal breakage.

IPC / J-STD-020D Reflow Specification

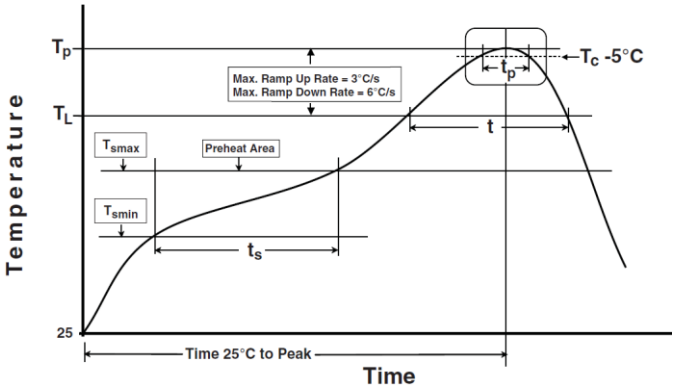
SnPb Classification Temperature		
Package Thickness	Volume mm³ <350	Volume mm³ ≥350
<2.5mm	235˚C	220˚C
≥2.5mm	220˚C	220˚C

Pb Free Classification Temperature			
Package Thickness	Volume mm³ <350	Volume mm³ 350 – 2000	Volume mm³ >2000
<1.6mm	260˚C	260˚C	260˚C
1.6mm – 2.5mm	260˚C	250˚C	245˚C
>2.5mm	250˚C	245˚C	245˚C

Reflow profiles in this document are for recommended limits. Actual board assembly profiles should be developed based on specific process needs and board designs, and should not exceed the parameters in the tables above.

We cannot give a definitive profile of the actual peak temperatures, as this is dependent on a number of factors which can only be decided by the assembler – the type of solder used, the size, specification and arrangement of other components on the board, and the overall thermal mass of the board.

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100˚C 150˚C 60 – 120 seconds	 150˚C 200˚C 60 – 120 seconds
Average ramp-up rate (T_{smax} to T_p)	3˚C/second max	3˚C/second max
Liquidous temperature (T_L) Time at liquidous (t_L)	183˚C 60 – 150 seconds	217˚C 60 – 150 seconds
Peak package body temperature (T_p)	See classification in temp Table above	See classification in temp Table above
Time (t_p) within 5˚C of the specified classification temperature (T_c)	20 seconds	30 seconds
Average ramp-down rate (T_p to T_{smax})	6˚C/second max.	6˚C/second max.
Time 25˚C to peak temperature	6 minutes max.	8 minutes max.



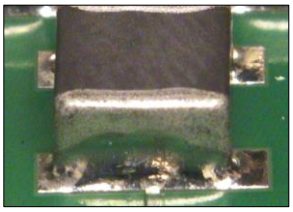
Unplated solderable silver ('8') termination

Note that Hiteca™ parts with unplated solderable silver ('8') termination have been designed specifically for conventional hot air reflow soldering.

Other reflow techniques, such as vapour phase or IR heating may also be suitable for these parts. However wave, drag or dip soldering techniques are not approved and these parts should not be immersed in molten solders.

The strength of unplated solderable silver termination matches or exceeds the termination strength of FlexiCap™ when tested for push force per AEC-Q200.

It should be noted that the use of a solderable leach-resistant silver termination can result in a different visual aspect to the solder joint - this is normal and acceptable.



Wave soldering

The thermal stresses caused by wave soldering have been shown to lead to potential problems with larger or thicker chips. For this reason, particular care should be taken when soldering SM chips larger than size 1210 and with a thickness greater than 1.0mm.

The MLCCs in the Hiteca™ range are large case size, thicker parts, and as such are not generally considered suitable for wave soldering applications.

Hand Soldering

Hand soldering is not recommended for MLCCs as the thermal stresses involved can result in micro-cracks forming in the dielectric material. These micro-cracks may develop with time and could ultimately result in electrical failure of the chip.

If hand soldering or solder touch up is considered necessary, it is important not to allow the iron tip to come into direct contact with the chip capacitor, but rather it should be applied to the pad adjacent to the capacitor and the heat allowed to soak gradually into the chip.

Minimise the rework heat duration, and allow components to cool naturally after soldering. Do not force cool as this can induce cracking. Ensure components are at room temperature before any cleaning process.

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Cleaning

Parts can be cleaned using rinse, spray or gentle ultrasonic agitation. Aggressive ultrasonics can cause damage to the dielectric or termination material, and could (for example) result in termination being removed.*

Solvent ultrasonic cleaning tends to be less aggressive than water based ultrasonic cleaning, as the ultrasonic energy is transmitted more efficiently by the water. Trials are recommended to ensure that the component is compatible with any preferred cleaning operation.

* Termination removal on the wrap around band may be acceptable as it will not impact form, fit or function. Termination removal on the end of the MLCC is not acceptable as reliability could be impacted.

Handling & Storage

Components should never be handled with fingers; perspiration and skin oils can inhibit solderability and will aggravate cleaning.

Chip capacitors should never be handled with metallic instruments. Metal tweezers should never be used as these can chip the product and leave abraded metal tracks on the product surface. Plastic or plastic coated metal types are readily available and recommended – these should be used with an absolute minimum of applied pressure.

Incorrect storage can lead to problems for the user. Rapid tarnishing of the terminations, with an associated degradation of solderability, will occur if the product comes into contact with industrial gases such as sulphur dioxide and chlorine. Storage in free air, particularly moist or polluted air, can result in termination oxidation.

Packaging should not be opened until the MLCs are required for use. If opened, the pack should be re-sealed as soon as practicable. Alternatively, the contents could be kept in a sealed container with an environmental control agent.

Long term storage conditions, ideally, should be temperature controlled between -5 and +40°C and humidity controlled between 40% and 60% R.H.

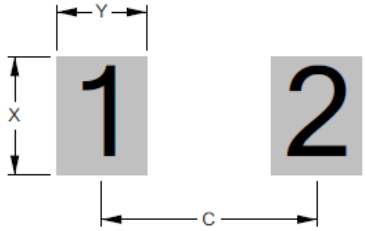
Taped product should be stored out of direct sunlight, which might promote deterioration in tape or adhesive performance.

Product, stored under the conditions recommended above, in its "as received" packaging, has a minimum shelf life of 2 years.

SM Pad Design

Knowles (Syfer) conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should also be considered.

IPC-7351 pad design



Mechanical Cracking considerations

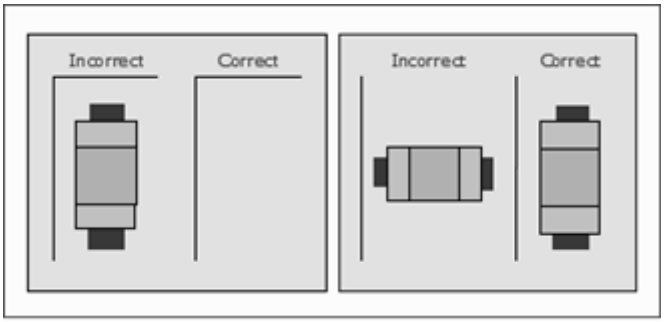
Mechanical cracking is one of the main causes of failure in MLCC's. Some design considerations can reduce the instances of mechanical cracking.

Assembly Design/ Manufacture Considerations

Mechanical stress can be influenced by a number of different factors associated with the design of the assembly and assembly manufacture. These factors include:

- PCB design – copper power and ground planes.
- A PCB design resulting in an uneven metal distribution (usually caused by large power or ground planes) can result in PCB warpage during the soldering process caused by the different Thermal Coefficient of Expansion rates between the copper and the epoxy fibre glass. If large power/ ground planes are required then cross hatching the copper area may prove to be useful.
- Position/ orientation of the capacitor on the PCB in relation to the edge of the PCB and other components/ attachments.

PCB Corner PCB Edge

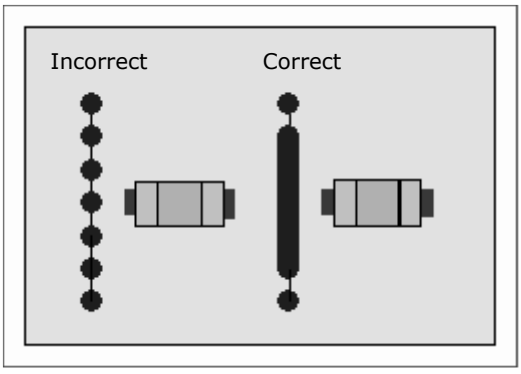


Capacitor placement not recommended in the corner of the PCB.

Recommended capacitor orientation with respect to PCB edge (denoted by black lines).

Note: Stress zone is typically within 5mm of PCB edge or fixing point.

Use of PCB Slots

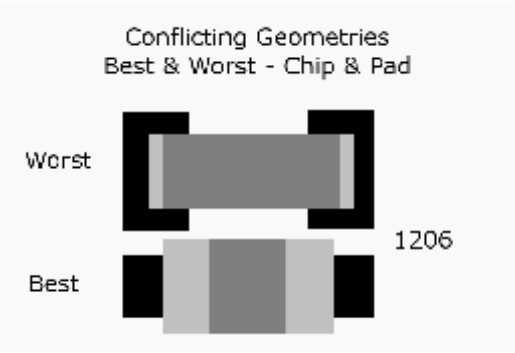


Using a slot along the depanelisation edge reduces the level of stress exerted onto the capacitor by approximately 50%.

	1206	1210	1812	1825	2220	2225
C	3.00 (0.118)	3.00 (0.118)	4.00 (0.157)	4.10 (0.161)	5.30 (0.209)	5.20 (0.205)
Y	1.15 (0.045)	1.15 (0.045)	1.55 (0.061)	1.45 (0.057)	1.50 (0.059)	1.65 (0.065)
X	1.80 (0.071)	2.70 (0.106)	3.40 (0.134)	6.80 (0.268)	5.40 (0.213)	6.70 (0.264)

All pad dimensions are in mm (inches)

Solder pad/ land sizes



Reducing the pad/land size can reduce the level of stress exerted onto the capacitor by approximately 50%.

Use of Adhesives

Depending upon the type of adhesive used, the effect can be a significant reduction in the bend strength of a capacitor. For example, during experiments approximately 50% of the PCB bend was required to crack a capacitor fixed with adhesive when compared to a capacitor not fixed with adhesive.

REACH (Registration, Evaluation, Authorisation and restriction of Chemicals) Statement

The main purpose of REACH is to improve the protection of human health and the environment from the risks arising from the use of chemicals.

Knowles maintain both ISO 14001 Environmental Management System, and OHSAS 18001 Health & Safety Management System approvals that require and ensure compliance with corresponding legislation such as REACH.

For further information, please contact your local sales office using the e-mail addresses at the front of this datasheet.

RoHS Compliance

Knowles routinely monitor world wide material restrictions (e.g., EU/China and Korea RoHS mandates) and is actively involved in shaping future legislation.

All standard Hiteca™, C0G/NP0, X7R, X5R and High Q Knowles MLCC products are compliant with the EU RoHS directive (see below for special exemptions), and those with plated terminations are suitable for soldering with common lead-free solder alloys (refer to 'Soldering Information' for more details on soldering limitations). Some, but not all, unplated terminations may also be compatible with lead-free solder alloys.

Compliance with EU RoHS directive automatically signifies compliance with some other legislation (e.g. Korea RoHS). Please refer to the Sales Office for details of compliance with other materials legislation.

Breakdown of material content, SGS analysis reports and tin whisker test results are available on request.

Most Knowles (Syfer) MLCC components are available with non-RoHS compliant tin/lead (SnPb) solderable termination finish for exempt applications and where pure tin is not acceptable. Other tin free termination finishes may also be available – please refer to the Sales Office for further details.

For the latest data, environmental certificates can be downloaded from www.knowlescapacitors.com

Export Controls and Dual-use Regulations

Certain Knowles catalogue components are defined as 'dual-use' items under international export controls – those that can be used for civil and military purposes which meet certain specified technical standards.

The defining criteria for a dual-use component with respect to Knowles products is one with a voltage rating >750Vdc, a capacitance value >250nF at 750Vdc, and a series inductance <10nH.

Components defined as 'dual-use' under the above criteria automatically require a licence for export outside the EU, and may require a licence for export with the EU.

The application for a licence is routine, but customers for these products will be asked to supply further information.

While all Hiteca™ parts have a series inductance of <10nH, none of the parts covered by this datasheet with a voltage rating of >750Vdc have a capacitance value of >250nF at 750Vdc.

This means that, currently, no Hiteca™ parts fall under the dual use regulations.

Note, however, that this may change in future as the Hiteca™ range is further extended.

If you require any further information on export controls or dual-use regulations, please contact the sales office.

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Ageing of Ceramic Capacitors

Capacitor ageing is a term used to describe the negative, logarithmic capacitance change which takes place in ceramic capacitors with time. The crystalline structure for barium titanate based ceramics changes on passing through its Curie temperature (known as the Curie Point) at about 125ºC. The domain structure relaxes with time and in doing so, the dielectric constant reduces logarithmically; this is known as the ageing mechanism of the dielectric constant. The more stable dielectrics have the lowest ageing rates.

The ageing process is reversible and repeatable. Whenever the capacitor is heated to a temperature above the Curie Point the ageing process starts again from zero.

The ageing constant, or ageing rate, is defined as the percentage loss of capacitance due to the ageing process of the dielectric which occurs during a decade of time (a tenfold increase in age) and is expressed as percent per logarithmic decade of hours. As the law of decrease of capacitance is logarithmic, this means that for a capacitor with an ageing rate of 1% per decade of time, the capacitance will decrease at a rate of:

a) 1% between 1 and 10 hours

b) An additional 1% between the following 10 and 100 hours

c) An additional 1% between the following 100 and 1000 hours

d) An additional 1% between the following 1000 and 10000 hours

e) The ageing rate continues in this manner throughout the capacitor's life.

Typical values of the ageing constant for our MLCCs are:

Dielectric Class	Typical Values
Hiteca™	Negligible capacitance loss through ageing
Ultra Stable C0G/NP0	Negligible capacitance loss through ageing
Stable X7R	<2% per decade of time

Capacitance Measurements

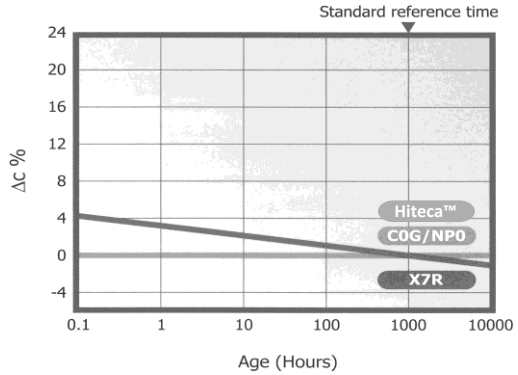
Because of ageing it is necessary to specify an age for reference measurements at which the capacitance shall be within the prescribed tolerance. This is fixed at 1000 hours, since for all practical purposes there is not much further loss of capacitance after this time.

All capacitors shipped are within their specified tolerance at the standard reference age of 1000 hours after having cooled through their Curie temperature.

The ageing curve for any ceramic dielectric is a straight line when plotted on semi-log paper.

Capacitance vs. Time

(Ageing X7R @ 1% per decade)



Tight Tolerance

One of the advantages of Knowles's unique 'wet process' of manufacture is the ability to offer capacitors with exceptionally tight capacitance tolerances.

The accuracy of the printing screens used in the fully automated, computer controlled manufacturing process allows for tolerance as close as ± 1% on C0G/NP0 parts greater than or equal to 10pF. For capacitance value less than 4.7pF tolerances can be as tight as ± 0.05pF.

Periodic Tests Conducted and Reliability Data

For standard surface mount capacitors, components are randomly selected on a sample basis and the following routine tests conducted:

- Load Test. 1,000 hours @ 125°C (150°C for X8R). Applied voltage depends on components tested
- Humidity Test. 168 hours @ 85°C/85%RH
- Board Deflection (bend test)

Test results are available on request.

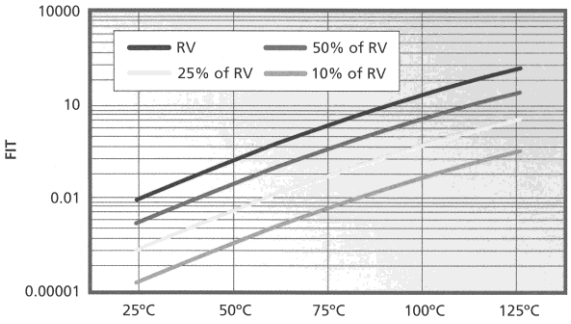
Conversion Factors

From	To	Operation
FITs	MTBF (hours)	10^9 ÷ FITs
FITs	MTBF (years)	10^9 ÷ (FITs × 8760)

FIT = Failures In Time. 1 FIT = 1 failure in 10^9 hours

MTBF = Mean Time Between Failure

Example of FIT Data Available



Component type: 0805 (C0G/NP0 and X7R)
Testing Location: Knowles reliability test department
Results based on: 16,622,000 component test hours

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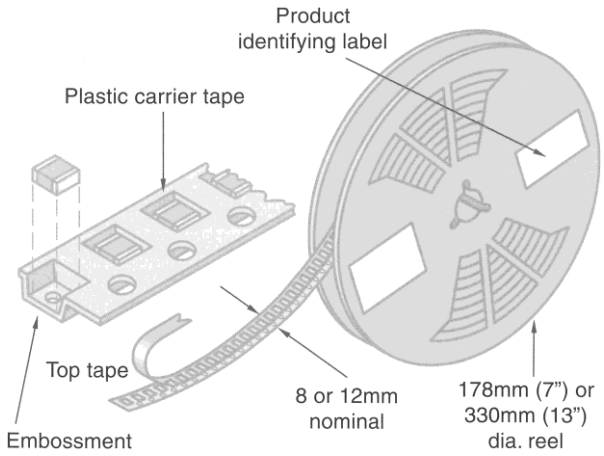
Packaging Information

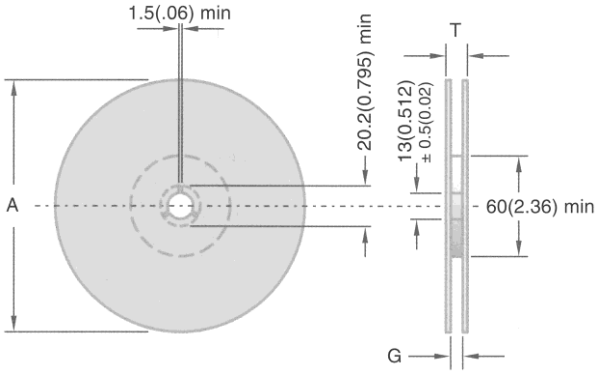
Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



Peel Force

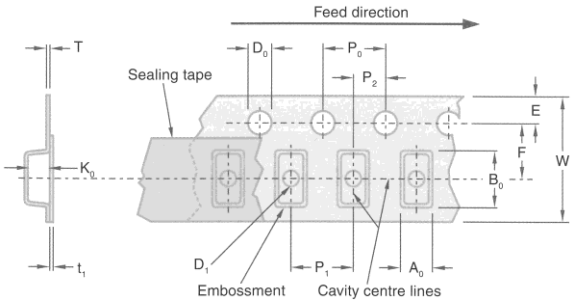
The peel force of the top sealing tape is between 0.2N and 1.0N at 180°. The breaking force of the carrier and sealing tape in the direction of unreeling is greater than 10N.

Reel Dimensions



Symbol	Description	178mm Reel	330mm Reel
A	Reel diameter	178 (7)	330 (13)
G	Reel inside width	8.4 (0.33)	12.4 (0.49)
T	Reel outside width	14.4 (0.56) max	18.4 (0.72) max

Tape Dimensions



		Dimensions mm (inches)	
Symbol	**Description**	**8mm Tape**	**12mm Tape**
A_0 B_0 K_0	Width of cavity Length of cavity Depth of cavity	Dependent on chip size to minimize rotation	
W	Width of tape	8.0 (0.315)	12.0 (0.472)
F	Distance between drive hole centres and cavity centres	3.5 (0.138)	5.5 (0.213)
E	Distance between drive hole centres and tape edge	1.75 (0.069)	
P_1	Distance between cavity centres	4.0 (0.156)	8.0 (0.315)
P_2	Axial distance between drive hole centres and cavity centres	2.0 (0.079)	
P_0	Axial distance between drive hole centres	4.0 (0.156)	
D_0	Drive hole diameter	1.5 (0.059)	
D_1	Diameter of cavity piercing	1.0 (0.039)	1.5 (0.059)
T	Carrier tape thickness	0.3 (0.012) ±0.1 (0.04)	0.4 (0.016) ±0.1 (0.04)
t_1	Top tape thickness	0.1 (0.004) max	

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Packing Information

Missing Components

The number of missing components in the tape may not exceed 0.25% of the total quantity with not more than three consecutive components missing. This must be followed by at least six properly placed components.

Identification

Each reel is labelled with the following information: manufacturer, chip size, capacitance, tolerance, rated voltage, dielectric type, batch number, date code and quantity of components.

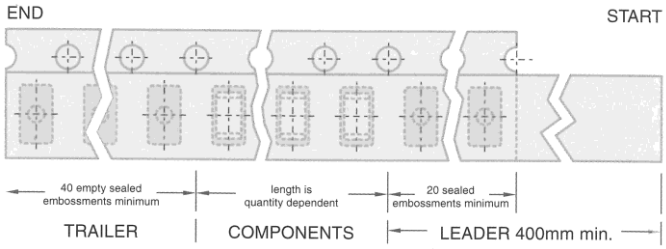
Component Orientation

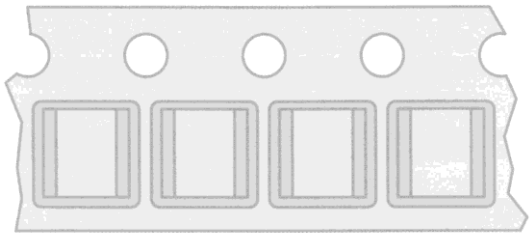
Tape and reeling is in accordance with IEC 60286 part 3, which defines the packaging specifications for leadless components on continuous tapes.

Notes: 1) IEC60286-3 states A0 <B0

2) Regarding the orientation of 1825 and 2225 components, the termination bands are right to left, NOT front to back. Please see diagram.

Leader Trailer



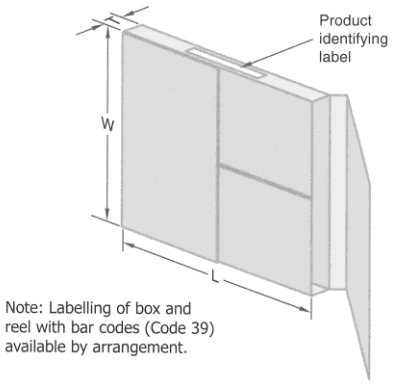


Orientation of 1825 & 2225 components

Outer Packaging

Outer carton dimensions mm (inches) max

Reel Size	No. of Reels	L	W	T
178 (7)	1	185 (7.28)	185 (7.28)	25 (0.98)
178 (7)	4	190 (7.48)	195 (7.76)	75 (2.95)
330 (13)	1	335 (13.19)	335 (13.19)	25 (0.98)



Note: Labelling of box and reel with bar codes (Code 39) available by arrangement.

Reel Quantities

Chip Size		1206	1210	1812	1825	2220	2225
Reel Quantities	178mm (7")	2500	2000	500	500	500	500
	330mm (13")	10000	8000	2000	2000	2000	2000

Notes:

1) The above quantities per reel are for the maximum manufactured chip thickness. Thinner chips can be taped in larger quantities per reel.

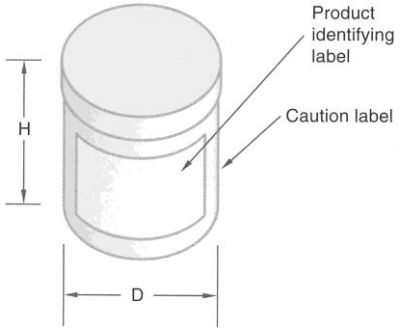
2) Where two different quantities are shown for the same case size, please contact the sales office to determine the exact quantity for any specific part number.

Bulk Packing – Tubs

Chips are supplied in rigid re-sealable plastic tubs together with impact cushioning wadding. Tubs are labelled with the details: chip size, capacitance, tolerance, rated voltage, dielectric type, batch number, date code and quantity of components.

Dimensions mm (inches)

H	60mm (2.36")
D	50mm (1.97")



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