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AMM-9024CH

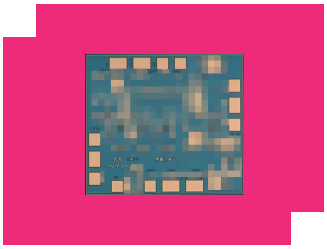
DC- 70GHz, Broadband Distributed Amplifier

DEVICE OVERVIEW

General Description

The AMM-9024CH is a broadband GaAs MMIC distributed amplifier enabling operation over a DC-70 GHz bandwidth. The amplifier features an 11 dB flat gain response, excellent return losses, and a low 2.5 dB noise figure. Available as a wire-bondable die.

Download s-parameters here



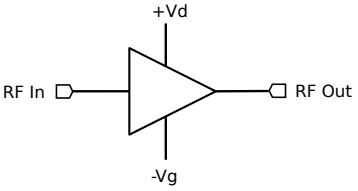
Features

- Ultra-broadband operation (DC-70GHz)
- Very flat gain response
- Excellent return losses

Applications

- Test and Measurement Equipment
- SATCOM
- LO signal chain for mmWave mixers
- Radar
- Electronic warfare equipment
- Aerospace and Defense

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
AMM-9024CH	DC- 70GHz, Broadband Distributed Amplifier	CH	REACH RoHS	Released	3A001.b.2.d

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Table Of Contents

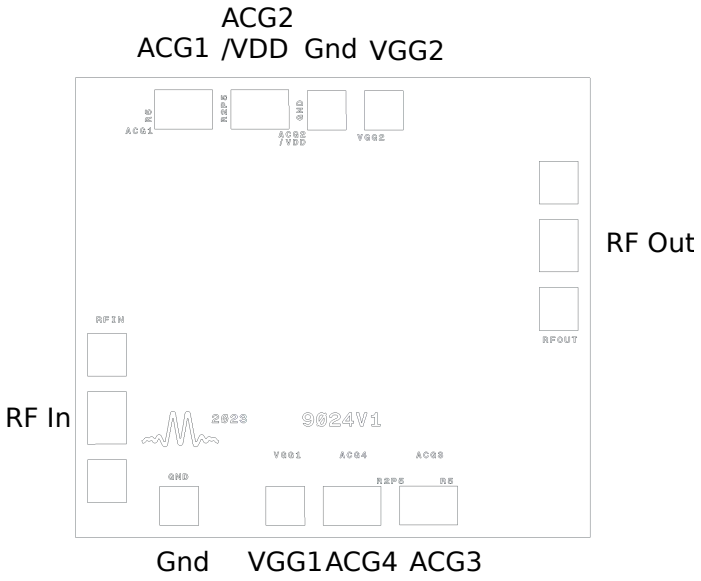
Revision History

Revision Code	Revision Date	Comment
-	2024-02-01	Initial Datasheet Release

Port Configuration and Functions

Port Diagram

The port diagram of the AMM-9024CH is shown below.



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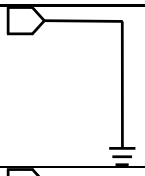
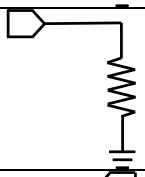
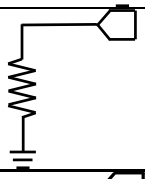
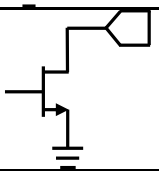
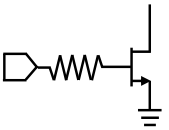
Port Functions

Port	Function	Description	Equivalent Circuit for Package
ACG1	AC Ground	This pad should be attached to an off-chip bypass capacitor. The recommended bypassing for this pad is 0.1uF. Do not ground this pad.	-
ACG3	AC Ground	This pad should be attached to an off-chip bypass capacitor. The recommended bypassing for this pad is 0.1uF. Do not ground this pad.	-
ACG4	AC Ground	This pad should be attached to an off-chip bypass capacitor. The recommended bypassing for this pad is 0.1uF. Do not ground this pad.	-
GND	Ground	Bottom side of the die must be connected to a DC/RF ground with high thermal and electrical conductivity. There is no need to bond to the Gnd pads on the top of the die.	
RF In	RF Input	The amplifier's RF Input pad, this pad requires an external blocking capacitor as shown in the application schematic. This pad is internally matched to 50 Ohms.	
RF Out	RF Output	The amplifier's RF Output pad, this pad requires an external blocking capacitor as shown in the application schematic. This pad is internally matched to 50 Ohms.	
VDD/ACG2	Drain Supply Voltage	This pad provides DC power to the drain of the amplifier. DC voltage at this pin should be set to 5V for normal operation.	
VGG1	Gate Bias Voltage	This pad provides DC bias to the gate of the amplifier. This pin requires a negative bias voltage for normal operation. The drain current Id of the amplifier will be controlled by the voltage applied to this pin. As this voltage becomes more positive, drain current will increase. For normal operation, the voltage on this pin should be set to produce a drain current of 45mA.	
VGG2	AC Ground	This pad should be attached to an off-chip bypass capacitors. The recommended bypassing for this pad is a 0.1uF+100pF. Do not ground this pad.	-

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Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime. Reliability limits are individual, instantaneous catastrophic limits only. Functional operation limits are indicated below. Operation of the device at multiple absolute maximum limits or for extended periods at a single limit can cause degradation and damage to the device.

Parameter	Maximum Rating	Unit
Drain Supply Voltage (Vd)	7	V
Gate Supply Voltage (Vg)	-1.5	V
Maximum Operating Temperature for MTTF > 1E6 hours	85	°C
Maximum Storage Temperature	125	°C
Minimum Operating Temperature for MTTF > 1E6 hours	-40	°C
Minimum Storage Temperature	-65	°C
Positive Drain Supply Current (Id) (with RF Input)	70	mA
RF Input Power	15	dBm

Package Information

Parameter	Details	Rating
Dimensions	-	1.35 x 1.2 mm

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the Electrical Specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Positive DC Current (Id) (No RF Input) [1]	-	45	-	mA
Input Power for Saturation	-	5	-	dBm
Gate Bias DC Voltage (Vg)	-	-0.25	-	V
Positive DC Voltage (Vd)	-	5	-	V

[1] Recommended operating current condition without RF input applied.

Sequencing Requirements

Turn-on Procedure:
1: Apply Vg = -0.5V (VGG1 pad)
2: Apply Vd voltage (VDD/ACG2 pad)
3: Increase Vg voltage towards -0.25V to achieve Id=45mA.
4: Apply RF input Power
Turn-off Procedure:
1: Turn off RF input Power
2: Turn off Vd voltage (VDD/ACG2 pad)
3: Turn off Vg voltage (VGG2 pad)

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Electrical Specifications

Unless otherwise specified, electrical specifications apply at TA=+25°C, Vd = 5V and Vg set such that Id = 45mA.

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Small Signal Gain	Vd=5V, Id=45mA, Pin=-20dBm	0	60	10	11.5	-	dB
Noise Figure	Vd=5V, Id=45mA, Pin=-20dBm	1	10	-	4	-	dB
Noise Figure	Vd=5V, Id=45mA, Pin=-20dBm	10	30	-	2.5	-	dB
Noise Figure	Vd=5V, Id=45mA, Pin=-20dBm	30	50	-	3	-	dB
Saturated Output Power	Vd=5V, Id=45mA (No RF applied)	0	30	12	14	-	dBm
Saturated Output Power	Vd=5V, Id=45mA (No RF applied)	30	60	8	11	-	dBm
Output P1dB	Vd=5V, Id=45mA (No RF applied)	0	30	-	11	-	dBm
Output P1dB	Vd=5V, Id=45mA (No RF applied)	30	60	-	8	-	dBm
Input Return Loss	Vd=5V, Id=45mA, Pin=-20dBm	0	60	-	20	-	dB
Output Return Loss	Vd=5V, Id=45mA, Pin=-20dBm	0	60	-	20	-	dB
Reverse Isolation	Vd=5V, Id=45mA, Pin=-20dBm	0	60	-	40	-	dB
Input Power for Saturation	Vd=5V, Id=45mA (No RF applied)	0	60	-	5	-	dBm

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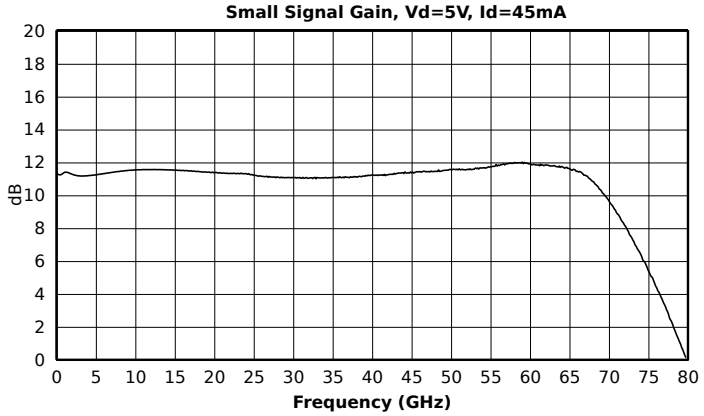
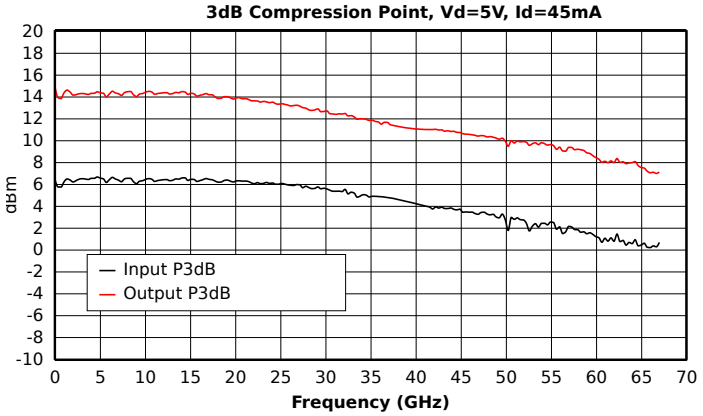
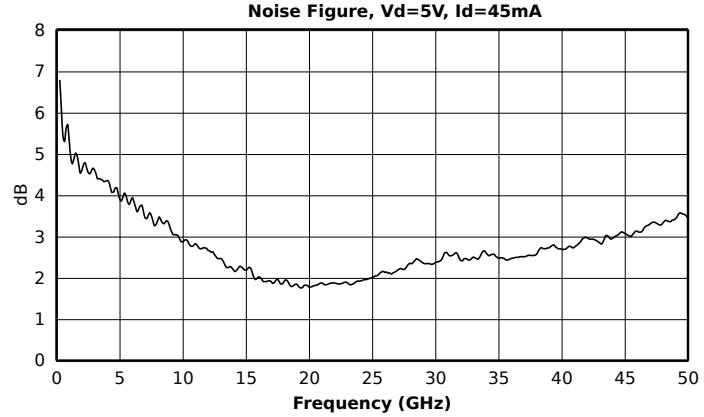
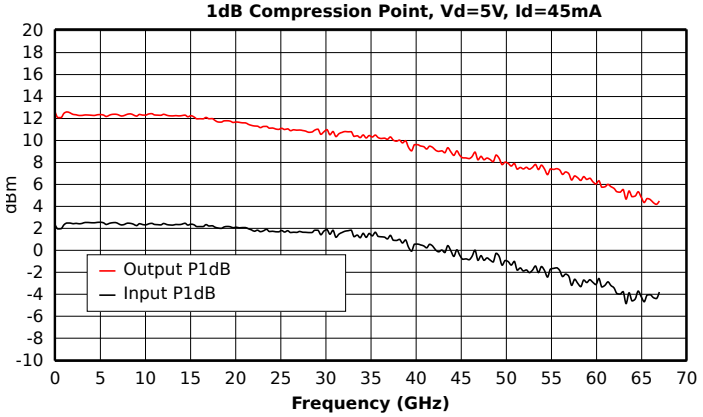
Performance plots measured using the recommended application circuit shown below.

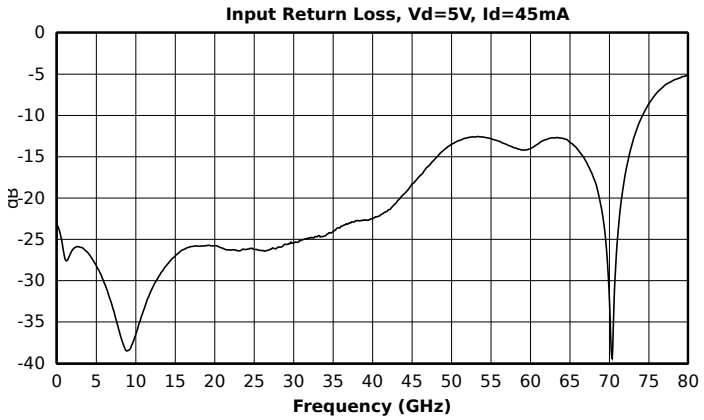
Typical Performance Plots

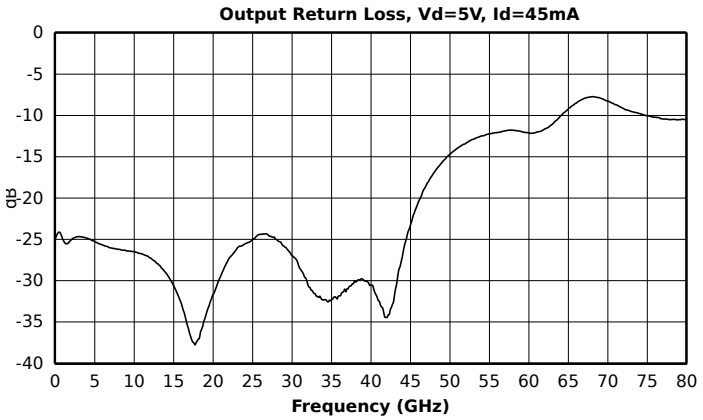


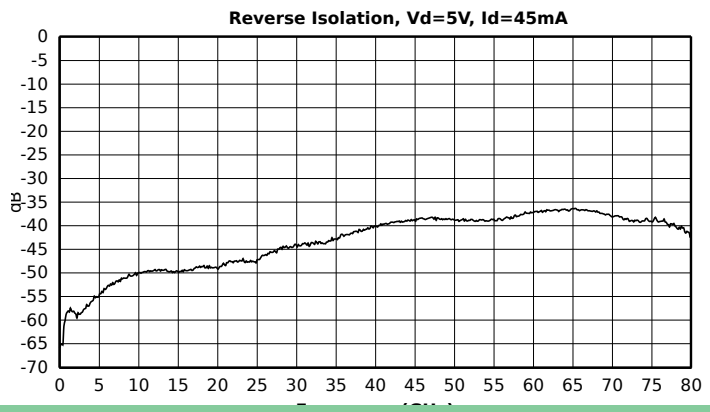












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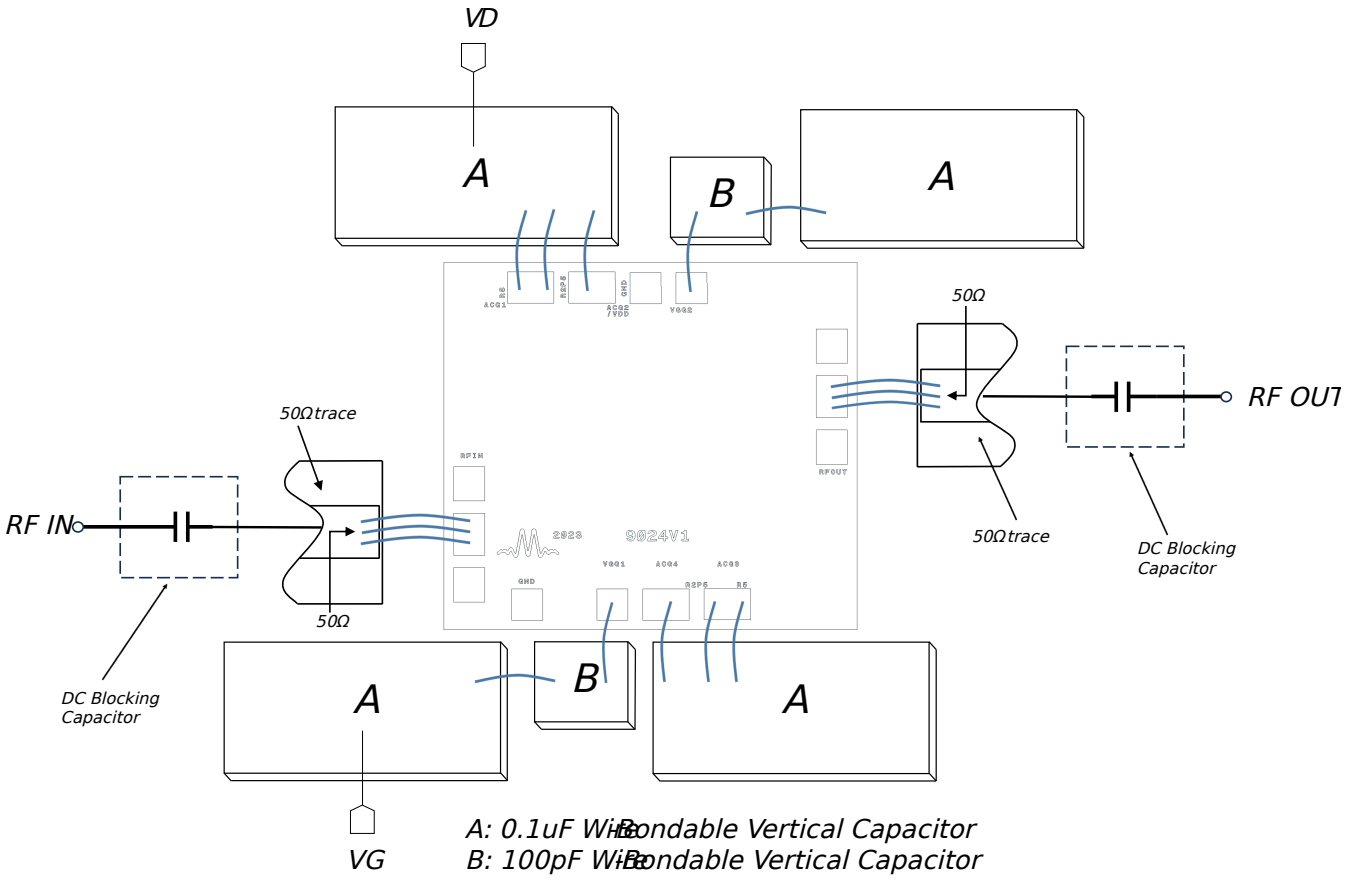
Application Circuit



A: 0.1uF Wirebondable Vertical Capacitor
B: 100pF Wirebondable Vertical Capacitor

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Application Circuit Description

Above is the recommended application circuit for the AMM-9024CH. Multiple DC power supply bypassing capacitors are shown around the die. These capacitors are of the vertical wire-bondable type. Type "A" capacitors are 0.1uF and type "B" capacitors are 100pF. DC drain voltage is supplied to the amplifier across a 0.1uF bypass capacitor to the VDD/AGC2 pad. DC gate bias voltage is supplied to the VGG2 pad across a 0.1uF+100pF bypass capacitor combination. In addition to bypass capacitors on the VDD/ACG2 and VGG2 pads, additional bypassing is recommended off the ACG4, ACG3 and VGG2 pads. 50 Ohm RF input and output traces should be bonded to the AMM-9024CH using 3 bondwires as shown in the diagram below. DC blocking capacitors are required at the input and output RF ports of the amplifier.

Die Mounting Recommendations

Mounting and Bonding Recommendations

Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This willprevent resonances and permit the best possible electrical performance. Datasheetperformance is only guaranteed in an environment with a low electrical impedance ground.

Mounting - To epoxy the chip, apply a minimum amount of conductive epoxy to themounting surface so that a thin epoxy fillet is observed around the perimeter of the chip.Cure epoxy according to manufacturer instructions.

Wire Bonding - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire.Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bondingforce of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Usethe minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should bestarted on the chip and terminated on the package or substrate. Bond wire inductancewill improve return loss. Bondwire inductance in the range of 30pH to 200pH will improveperformance.

Circuit Considerations – 50 Ω transmission lines should be used for all high frequencyconnections in and out of the chip. Wirebonds should be kept as short as possible, withmultiple wirebonds recommended for higher frequency connections to reduce parasiticinductance. In circumstances where the chip more than .001” thinner than thesubstrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

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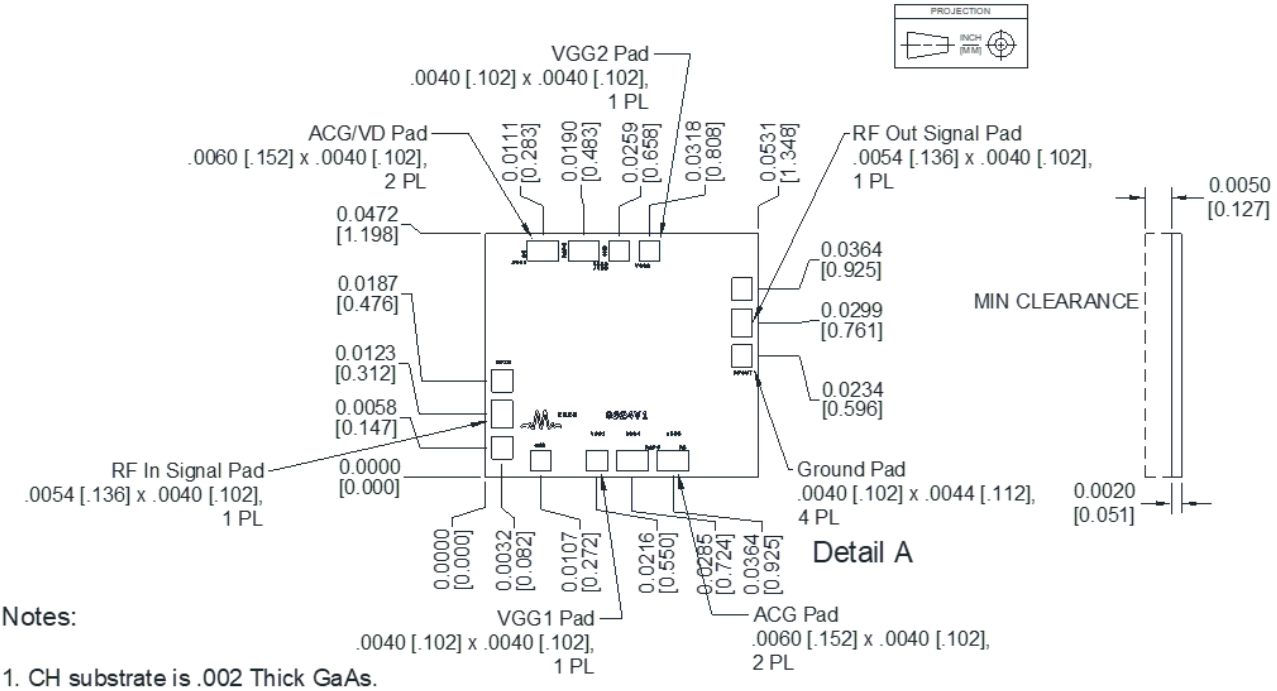
Mechanical Data

Outline Drawing

Download : Outline 2D Drawing



Notes:

1. CH substrate is .002 Thick GaAs.
2. I/O trace is 3 microns and ground plane is 4 microns Au.
3. Tolerance for X, Y dimensions is ± 0.002 in.
   Tolerance for Z dimension is ± 0.0005 in.
   Tolerance for pad location is ± 0.0001 in.

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DISCLAIMER