
PXle-1487

Specifications

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This document lists the specifications for the following variants of the PXle-1487:

- PXle-1487 FlexRIO GMSL2 Deserializer modules
- PXle-1487 FlexRIO GMSL2 Serializer modules
- PXle-1487 FlexRIO GMSL2 SerDes modules



Note If you purchased the PXle-1487 as part of an NI system, refer to your system documentation for application-specific specifications.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Specifications are **Typical** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 23 °C ±5 °C



- Installed in chassis with slot cooling capacity $\geq 58 \text{ W}^1$

PXle-1487 Pinout

Deserializer Pinout

Figure 1. Deserializer Front Panels

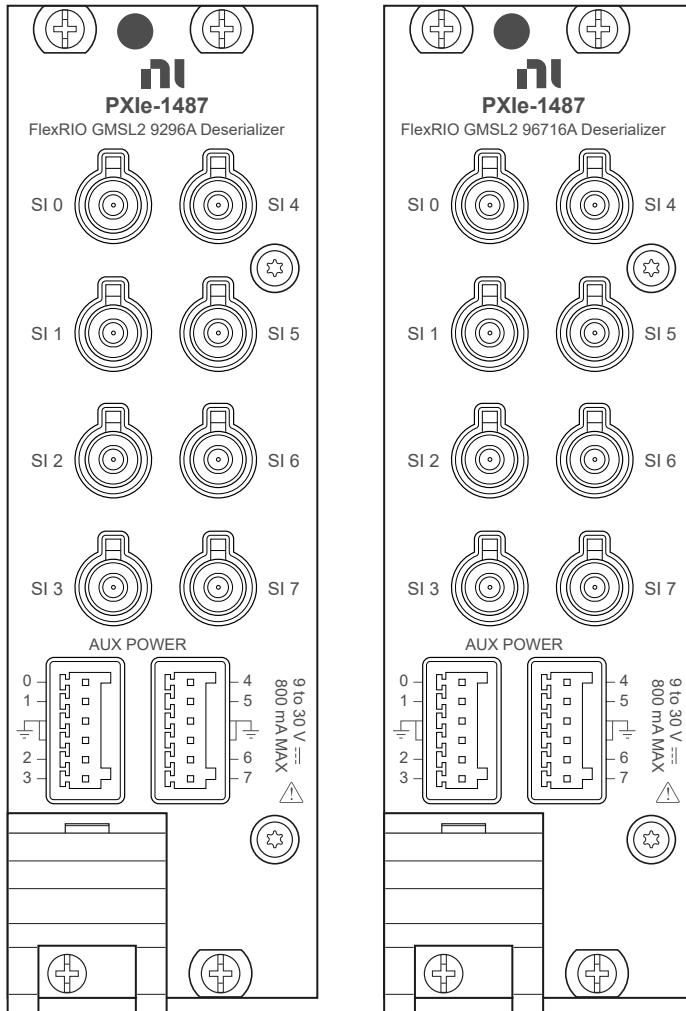


Table 1. Deserializer Front Panel Connectors Signal Descriptions

Signal Name	Description	FlexRIO Terminal Name
SI 0	Serial input to internal deserializer	SI0
SI 1	Serial input to internal deserializer	SI1
SI 2	Serial input to internal deserializer	SI2

1. The PXle-1487 SerDes module can operate in a chassis with a slot cooling capacity of $< 58 \text{ W}$ in a restricted user mode.

Signal Name	Description	FlexRIO Terminal Name
SI 3	Serial input to internal deserializer	SI3
SI 4	Serial input to internal deserializer	SI4
SI 5	Serial input to internal deserializer	SI5
SI 6	Serial input to internal deserializer	SI6
SI 7	Serial input to internal deserializer	SI7

Figure 2. Deserializer AUX Power Connectors

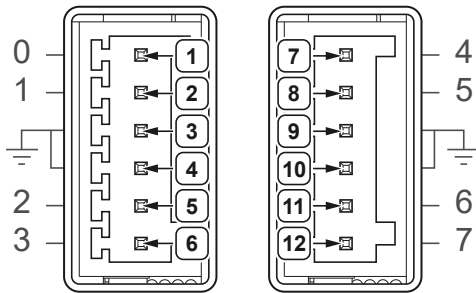


Table 2. Deserializer AUX Power Connectors Signal Descriptions

Signal Pin	Description
1	Power supply for channel SI 0
2	Power supply for channel SI 1
3	Digital/chassis grounding
4	Digital/chassis grounding
5	Power supply for channel SI 2
6	Power supply for channel SI 3
7	Power supply for channel SI 4
8	Power supply for channel SI 5
9	Digital/chassis grounding
10	Digital/chassis grounding
11	Power supply for channel SI 6
12	Power supply for channel SI 7

Serializer Pinout

Figure 3. Serializer Front Panels

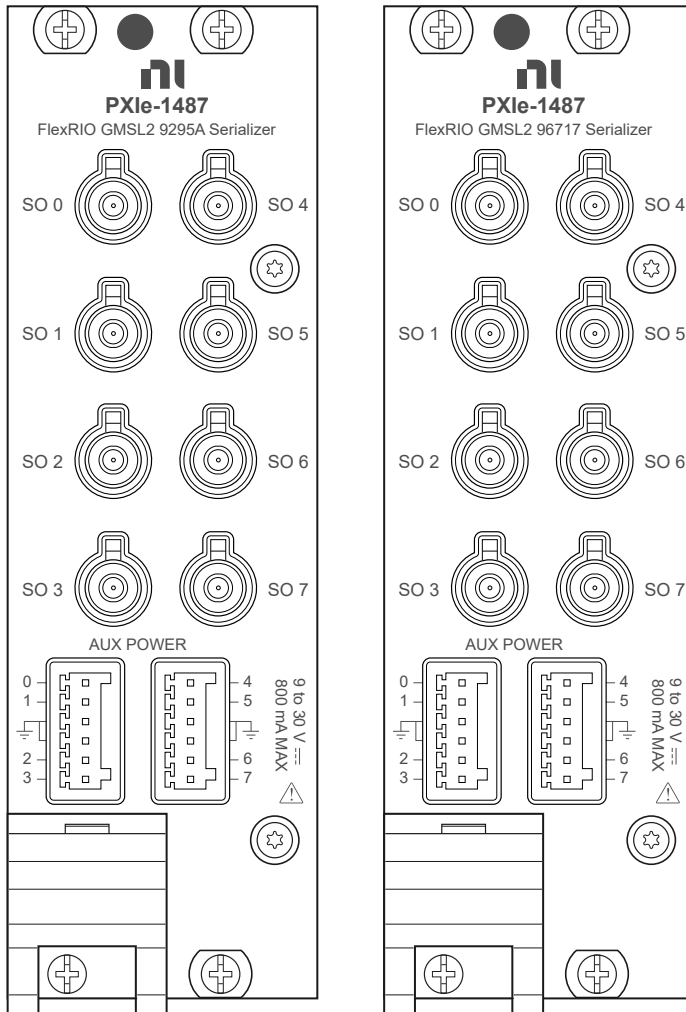


Table 3. Front Panel Connectors Signal Descriptions

Signal Name	Description	FlexRIO Terminal Name
SO 0	Serial output from internal serializer	SO0
SO 1	Serial output from internal serializer	SO1
SO 2	Serial output from internal serializer	SO2
SO 3	Serial output from internal serializer	SO3
SO 4	Serial output from internal serializer	SO4
SO 5	Serial output from internal serializer	SO5
SO 6	Serial output from internal serializer	SO6

Signal Name	Description	FlexRIO Terminal Name
SO 7	Serial output from internal serializer	S07

Figure 4. Serializer AUX Power Connectors

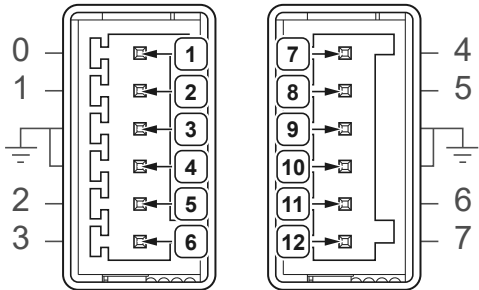


Table 4. AUX Power Connectors Signal Descriptions

Signal Pin	Description
1	Power sink for channel SO 0
2	Power sink for channel SO 1
3	Digital/chassis grounding
4	Digital/chassis grounding
5	Power sink for channel SO 2
6	Power sink for channel SO 3
7	Power sink for channel SO 4
8	Power sink for channel SO 5
9	Digital/chassis grounding
10	Digital/chassis grounding
11	Power sink for channel SO 6
12	Power sink for channel SO 7



SerDes Pinout

Figure 5. SerDes Front Panels

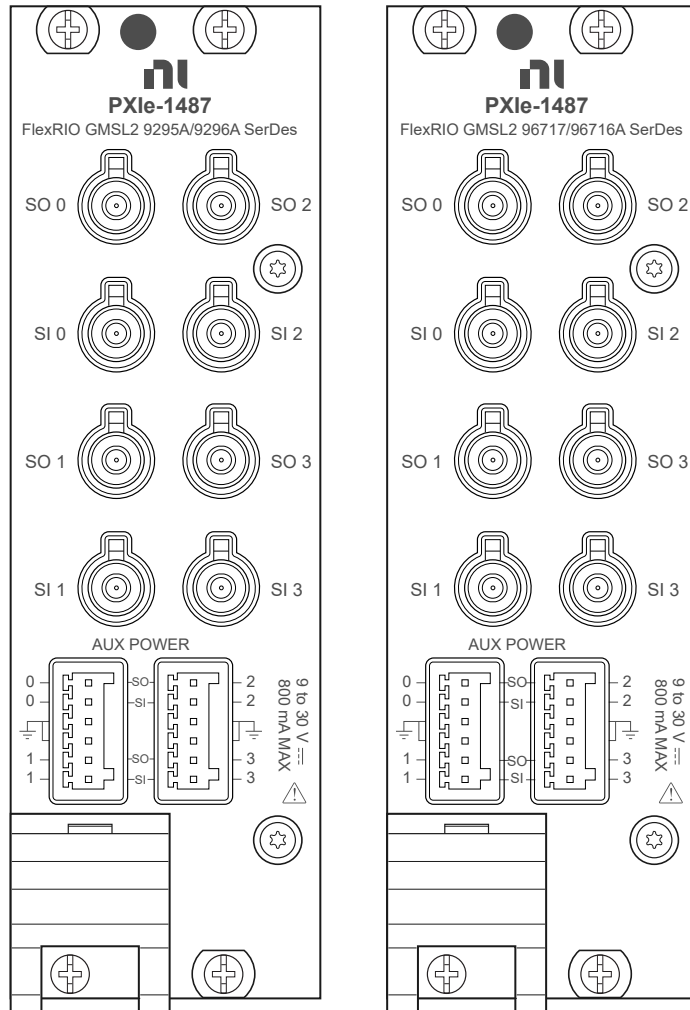


Table 5. Front Panel Connectors Signal Descriptions

Signal Name	Description	FlexRIO Terminal Name
SO 0	Serial output from internal serializer	SO0
SI 0	Serial input to internal deserializer	SI0
SO 1	Serial output from internal serializer	SO1
SI 1	Serial input to internal deserializer	SI1
SO 2	Serial output from internal serializer	SO2
SI 2	Serial input to internal deserializer	SI2
SO 3	Serial output from internal serializer	SO3

Signal Name	Description	FlexRIO Terminal Name
SI 3	Serial input to internal deserializer	SI3

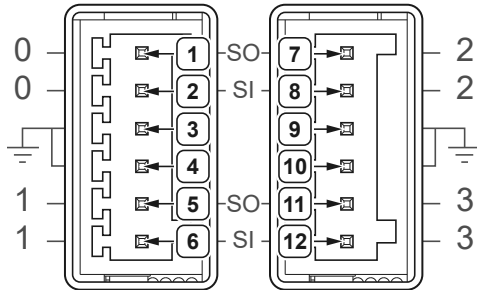


Figure 6. SerDes AUX Power Connectors

Table 6. AUX Power Connectors Signal Descriptions

Signal Pin	Description
1	Power sink for channel SO 0
2	Power supply for channel SI 0
3	Digital/chassis grounding
4	Digital/chassis grounding
5	Power sink for channel SO 1
6	Power supply for channel SI 1
7	Power sink for channel SO 2
8	Power supply for channel SI 2
9	Digital/chassis grounding
10	Digital/chassis grounding
11	Power sink for channel SO 3
12	Power supply for channel SI 3

Serial Device Compatibility

Refer to the following information to verify that the PXle-1487 module chip set is compatible with your serial device or camera.

Chip set brand	Maxim Integrated
Module deserializer	MAX9296A
Module serializer	MAX9295A



Note Contact the manufacturer of your serial device or camera for details on compatibility with the PXle-1487 module.

PXle-1487 Variant Mode Support

Refer to the following to verify whether your PXle-1487 variant supports Pixel or Tunneling Mode.

Table 7. PXle-1487 Variants

PXle-1487 Variant	Serializer	Deserializer	Mode Supported
GMSL2 Interface Module, 8 In, MAX96716A Deserializers	N/A	MAX96716A	Tunneling and Pixel
GMSL2 Interface Module, 8 Out, MAX96717 Serializers	MAX96717	N/A	Tunneling and Pixel
GMSL2 Interface Module, 4 In 4 Out, MAX96717/MAX96716A SerDes	MAX96717	MAX96716A	Tunneling and Pixel
GMSL2 Interface Module, 8 In, MAX9296A Deserializers	N/A	MAX9296A	Pixel
GMSL2 Interface Module, 8 Out,	MAX9295A	N/A	Pixel



PXle-1487 Variant	Serializer	Deserializer	Mode Supported
MAX9295A Serializers			
GMSL2 Interface Module, 4 In 4 Out, MAX9295A/MAX9296A SerDes	MAX9295A	MAX9296A	Pixel

Bus Interface

Form factor	PCI Express Gen-3 x8
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Reconfigurable FPGA

The following table lists the specifications for the PXle-1487 FPGA.

FPGA	KU11P
LUTs	298,560
DSP48 slices (25 × 18 multiplier)	2,928
Embedded Block RAM	21 Mb
Timebase reference sources	PXI Express 100 MHz (PXle_CLK100)
Data transfers	DMA, interrupts, programmed I/O

Embedded UltraRAM™	22 Mb
Number of DMA channels	60



Note These values reflect the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI support.

Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

Serial I/O Characteristics

Input Channels

Connector label	SI
Connector type	FAKRA Male Code Z, coaxial
PoC output range, AUX power maximum	9 V to 30 V, 800 mA per channel
PoC output range, internal power supply	
Nominal voltage	12 V
Maximum current	400 mA per channel, 2 A total
I/O standard	GMSL2 with power over coax (PoC)
Maximum data rate	6 Gb/s

Output Channels

Connector label	SO
Connector type	FAKRA Male Code Z, coaxial
PoC input range	

Nominal voltage	9 V to 30 V
Maximum current	800 mA per channel
I/O standard	GMSL2 with power over coax (PoC)
Maximum data rate	6 Gb/s

AUX Power Channels

Power sink or source maximum voltage	9 V to 30 V
Power sink or source maximum current	800 mA per channel
Power connector type	Conn Terminal Block, Weidmuller part number 2439690000
Power connector wiring	
Gauge	0.08 mm ² to 0.5 mm ² (28 AWG to 20 AWG)
Wire strip length	8 mm
Terminal connection type	Tension clamp

Retention	External strain relief of AUX power connections recommended
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PXle-1487 Deserializer

Input channels	8
Communication	I2C Configuration, I2C Backchannel, GPIO Communication, CSI-2
CSI-2 interface	4 lane, 1,200 Mbps per lane, no lane swaps or inversions

PXle-1487 Serializer

Output channels	8
Communication	I2C Configuration, I2C Backchannel, GPIO Communication, CSI-2
CSI-2 interface	4 lane, 1,200 Mbps per lane, no lane swaps or inversions

PXle-1487 SerDes

Input channels	4
Output channels	4
Maximum Tap pairs per module	4

Communication	I2C Configuration, I2C Backchannel, GPIO Communication, CSI-2
CSI-2 interface	4 lane, 1,200 Mbps per lane, no lane swaps or inversions

Power Requirements



Note Power requirements are dependent on the contents of the LabVIEW FPGA VI used in your application.



Note Do not position product so that it is difficult to disconnect power.



Note If you are powering the PXle-1487 using your PXle chassis backplane, refer to the chassis specifications for detailed information about your internal power supply.

Backplane Power Source

Backplane Power	
3.3 V	3.0 A, maximum
12 V	6.0 A, maximum

Total power	82 W, maximum
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Power over Coax (PoC) Source

External Power Supply	
Voltage range	9 V to 30 V
Maximum current	800 mA per channel, up to 8 channels

Internal Power Supply	
Nominal voltage	12 V
Maximum current	400 mA per channel, up to 2 A total

Diagnostic PoC Measurement	
Current measurement range	50 mA to 800 mA
Current measurement accuracy, 50 mA to 100 mA	±20%
Current measurement accuracy, 100 mA to 800 mA	±15%
Voltage measurement range	6 V to 32 V
Voltage measurement accuracy ²	5%

Environmental Characteristics

Table 8. Temperature

Operating	0 °C to 55 °C ³
Storage	-40 °C to 71 °C

Table 9. Humidity

Operating	10% to 90%, noncondensing
Storage	5% to 95%, noncondensing

Table 10. Pollution Degree

Pollution degree	2
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Table 11. Maximum Altitude

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
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- Due to resistive (IR drop) losses in the circuit, actual voltage measurement accuracy depends on the load of the PoC circuit.
- The PXIe-1487 requires a chassis with slot cooling capacity ≥ 58 W. Not all chassis with slot cooling capacity ≥ 58 W can achieve this ambient temperature range. Refer to PXI chassis specifications on ni.com/docs to determine the ambient temperature ranges your chassis can achieve.

Table 12. Shock and Vibration

Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse

Physical

Dimensions	3U, two-slot PXI Express module, 21.6 cm × 4.1 cm × 13.0 cm (8.5 in. × 1.6 in. × 5.1 in.)
Weight	692 g (24.38 oz)

Timing and Synchronization

Timebase	100 MHz, shared by all ports, disciplined by PXI_Clk100
Trigger I/O source	PXI_Trig <0:7>