

SuperQ™ 150V N-Channel Power MOSFET

FEATURES

- Industry leading $R_{DS(on)}$ in TOLL package
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production
- Low switching losses, Q_{sw} and E_{oss}
- 175°C temperature rating

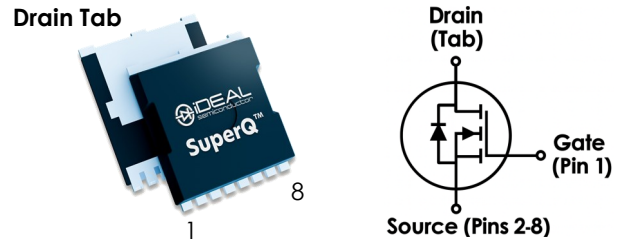
APPLICATIONS

- Motor control
- Battery disconnect switch
- Switch mode power on primary & secondary

DESCRIPTION

Engineered for high-efficiency motor drives and battery disconnect switches, this 150V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust TOLL package. Featuring best-in-class $R_{DS(on)}$, Q_{sw} and short-circuit handling, it minimizes heat dissipation at both full and partial loads.

PRODUCT SUMMARY



TOLL

Parameter	Value	Unit
$T_A = 25^\circ\text{C}$		
V_{DS}	150	V
$R_{DS(on),max}$	2.5	m Ω
I_D	233	A
Q_G	123	nC
Q_{sw}	8.9	nC
E_{oss}	2.6	μJ



ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS15M2R5S1T	TOLL	iS15M2R5S1	13' 2,000pcs T&R

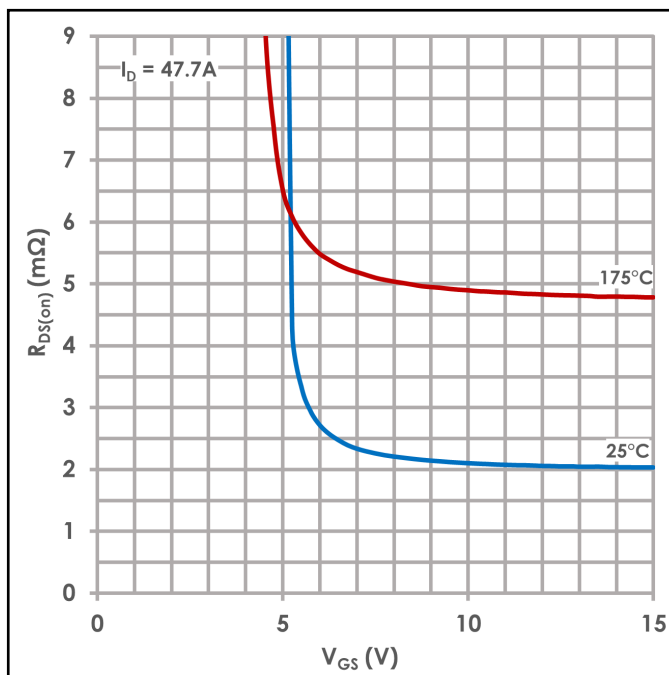


Figure 1: Typical Drain-Source On Resistance

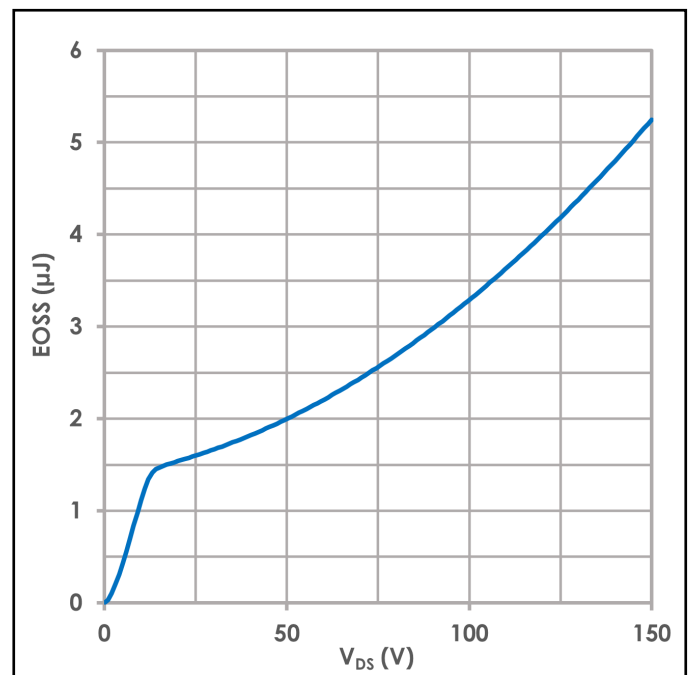


Figure 2: Typical C_{oss} Stored Energy



ABSOLUTE MAXIMUM RATINGS			
SYMBOL	PARAMETER (T _A = 25°C unless otherwise specified)	VALUE	UNIT
V _{GS}	Gate-to-source voltage	± 20	V
I _D	Continuous drain current (silicon limited), T _C = 25°C	233	A
	Continuous drain current (silicon limited), T _C = 100°C	165	
I _{DM}	Pulsed drain current	829	A
P _D	Power dissipation, T _C = 25°C	314	W
T _J , T _{stg}	Operating junction, storage temperature	-55 to 175	°C
E _{AS}	Avalanche energy, single pulse I _D = 48.4A, R _{GS} = 25Ω	1,171	mJ

THERMAL CHARACTERISTICS					
SYMBOL	PARAMETER (T _A = 25°C unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
R _{θJC}	Junction-to-case thermal resistance - TOLL	-	-	0.48	°C/W
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	-	-	50	°C/W

(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
B _V DSS	Drain-to-source voltage	V _{GS} = 0V, I _D = 1mA	150	-	-	V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0V, V _{DS} = 120V, T _J = 25°C	-	0.2	1	μA
		V _{GS} = 0V, V _{DS} = 120V, T _J = 125°C ⁽²⁾	-	-	100	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0V, V _{GS} = 20V	-	1	100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 321μA	2.5	3.3	4.1	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 10V, I _D = 47A	-	2.0	2.5	mΩ
		V _{GS} = 8V, I _D = 24A	-	2.2	2.8	
g _{fs}	Transconductance	V _{DS} = 10V, I _D = 47A	107	215	-	S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance ⁽²⁾	V _{GS} = 0V, V _{DS} = 75V, f = 100kHz	-	7,560	9,828	pF
C _{rss}	Reverse transfer capacitance ⁽²⁾		-	58	75	
C _{oss}	Output capacitance ⁽²⁾		-	344	447	
C _{o(er)}	Effective output capacitance	V _{DS} = 0 to 75V, V _{GS} = 0V	-	458	-	
R _G	Series gate resistance	f = 1MHz	-	1.0	1.4	Ω
t _{d(on)}	Turn-on delay time	V _{DS} = 75V, V _{GS} = 10V, I _{DS} = 47A, R _{G,EXT} = 0 Ω	-	18.8	-	ns
t _r	Rise time		-	2.6	-	
t _{d(off)}	Turn-off delay time		-	50.0	-	
t _f	Fall time		-	4.9	-	
GATE CHARGE CHARACTERISTICS						
Q _g	Gate charge total ⁽²⁾	V _{DS} = 75V, I _D = 30A, V _{GS} = 0 to 10V	-	123	160	nC
Q _{sw}	Switching charge ⁽³⁾		-	8.9	-	
Q _{gd}	Gate to drain charge ^{(2) (3)}		-	4.9	6.4	
Q _{g(th)}	Gate charge at threshold ⁽³⁾		-	20.4	-	
Q _{gs2}	Gate to source charge ⁽³⁾		-	4.0	-	
V _{plateau}	Gate plateau voltage		-	5.2	-	V
Q _{oss}	Output charge ⁽²⁾	V _{DS} = 0 to 75V, V _{GS} = 0V	-	349	401	nC
E _{oss}	Capacitive stored energy		-	2.6	-	μJ
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 47A, V _{GS} = 0V	-	0.80	0.90	V
Q _{rr}	Reverse recovery charge	V _{DS} = 75V, I _F = 47A,	-	209	-	nC
t _{rr}	Reverse recovery time	di/dt = 100A/μs	-	111	-	ns

(2) Defined by design. Not subject to production test.

(3) Q_{sw} should be used for switching loss calculations. See Figure 16 for gate charge definitions. For more information see Q_{sw} application note on www.idealsemi.com



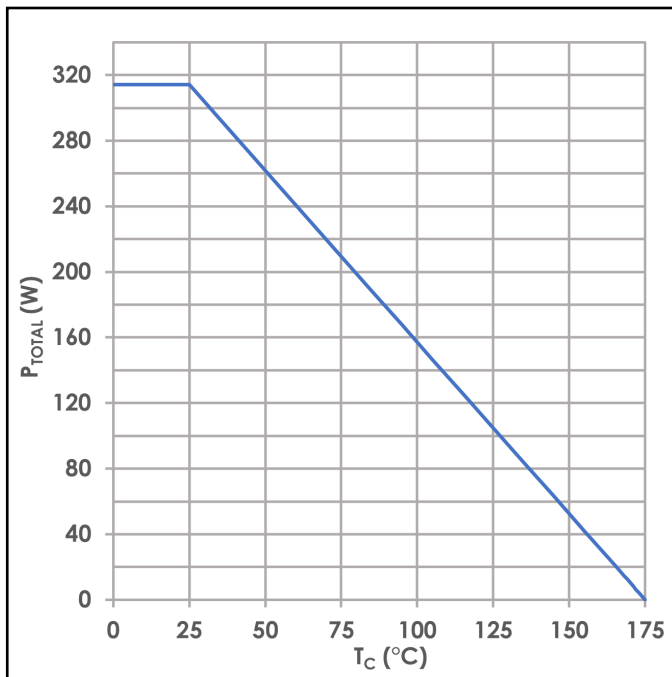


Figure 3: Power Dissipation

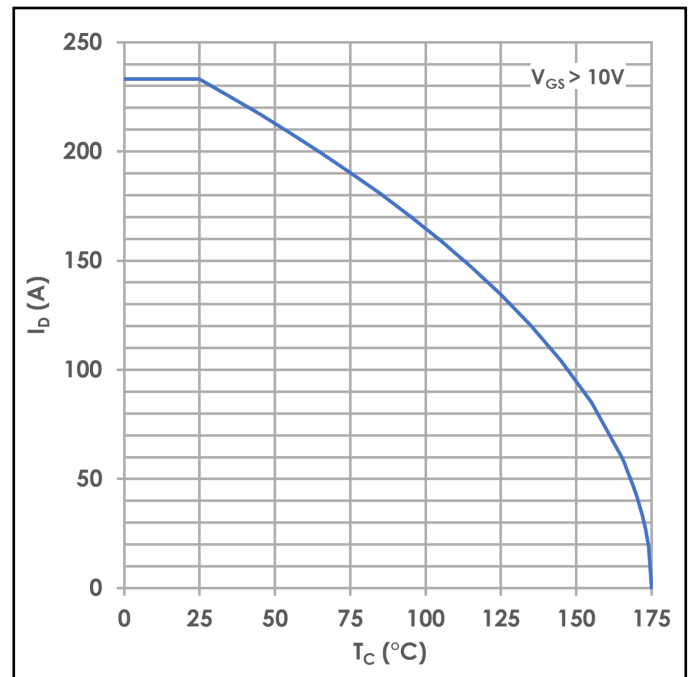


Figure 4: Drain Current

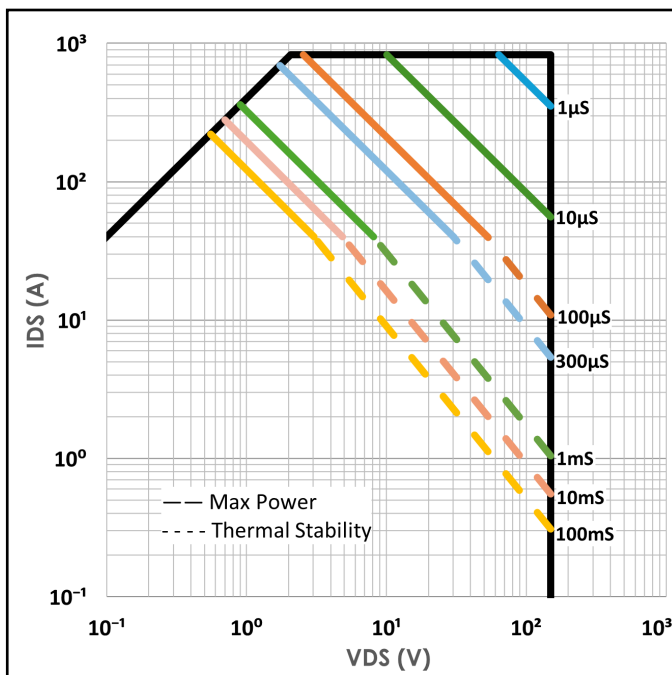


Figure 5: Safe Operating Area

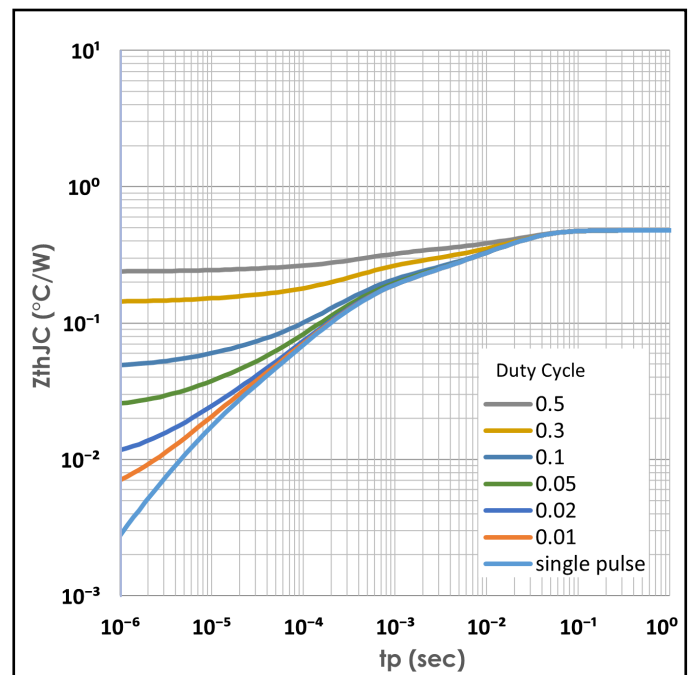


Figure 6: Max Transient Thermal Impedance

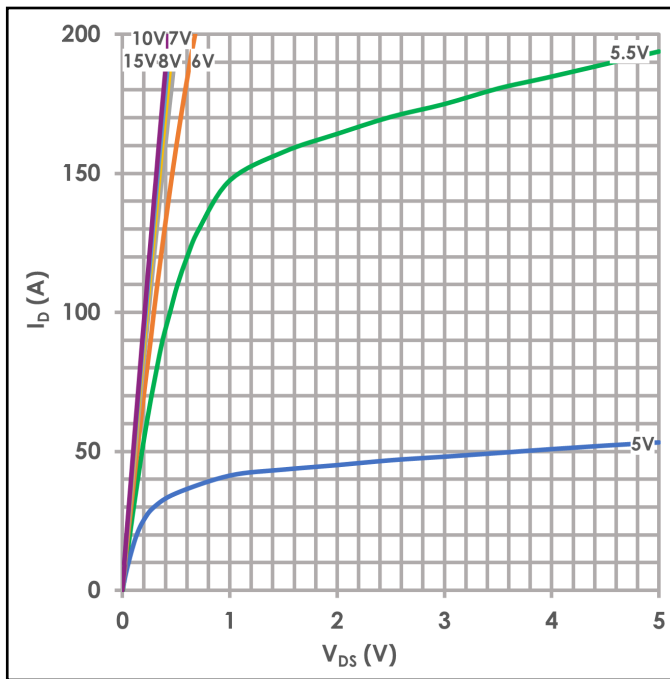


Figure 7: Typical Output Characteristics

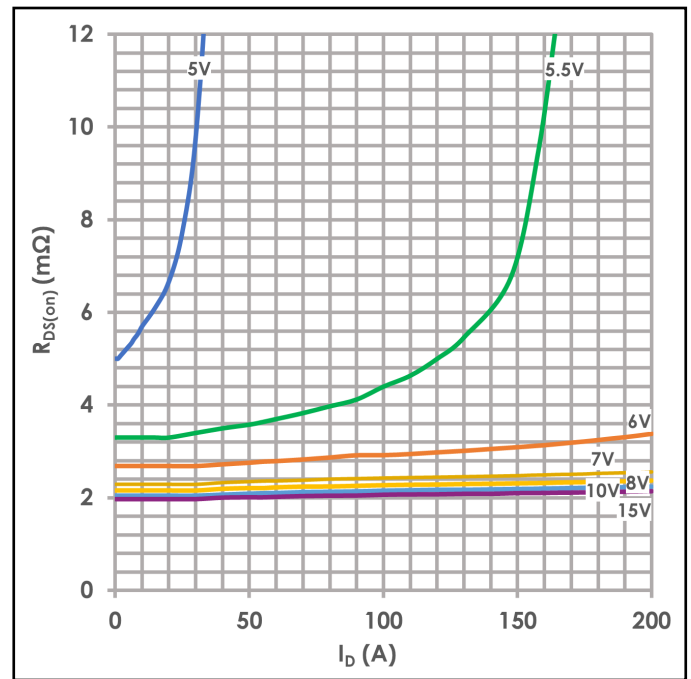


Figure 8: Typical Drain-Source On-Resistance

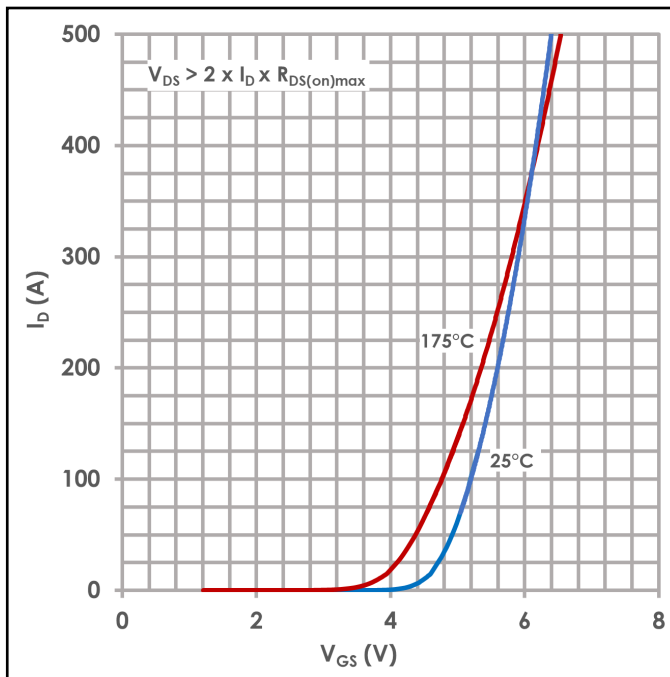


Figure 9: Typical Transfer Characteristics

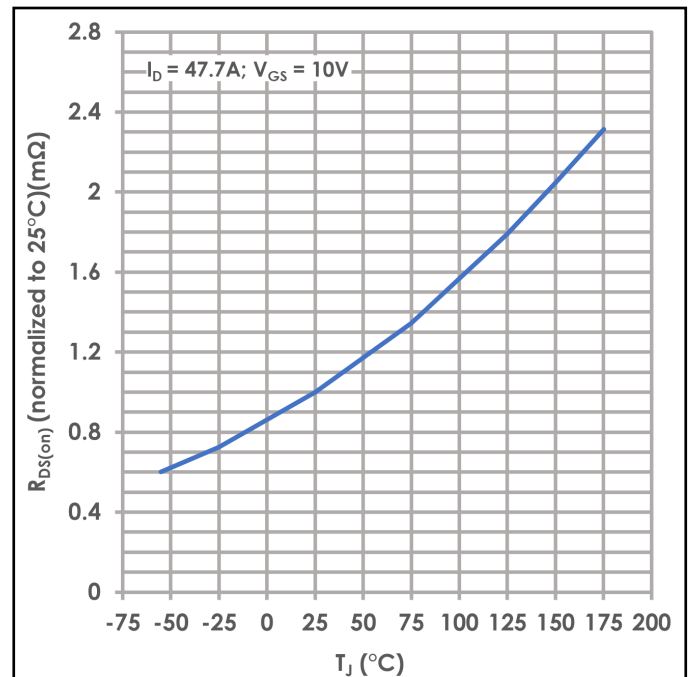


Figure 10: Normalized On-State Resistance vs. Temperature

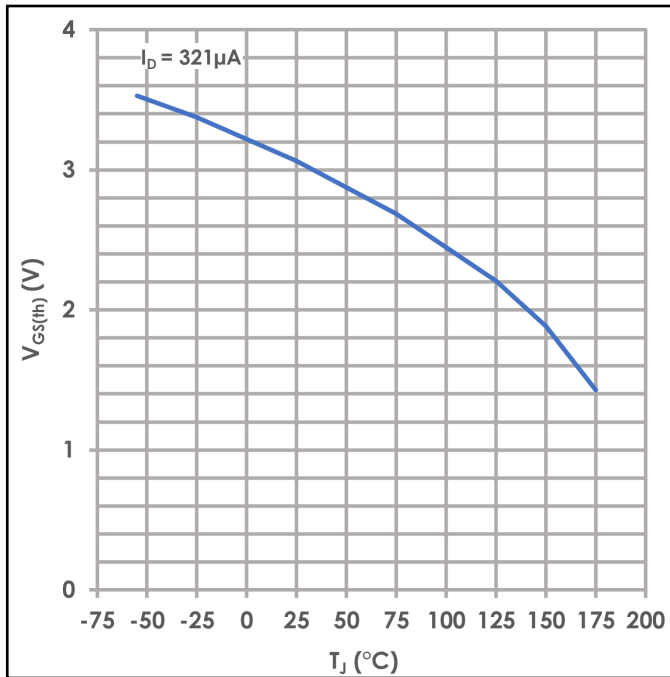


Figure 11: Typical Threshold Voltage

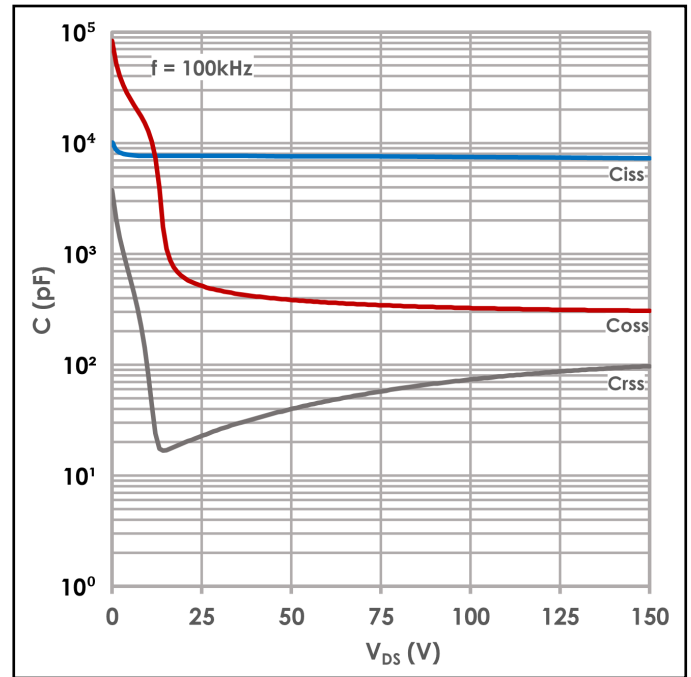


Figure 12: Typical Capacitances

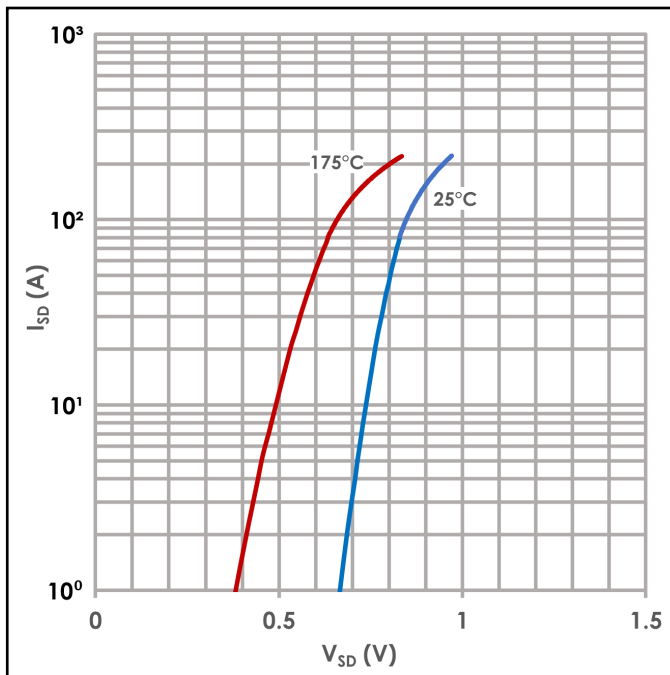


Figure 13: Typical Diode Forward Voltage

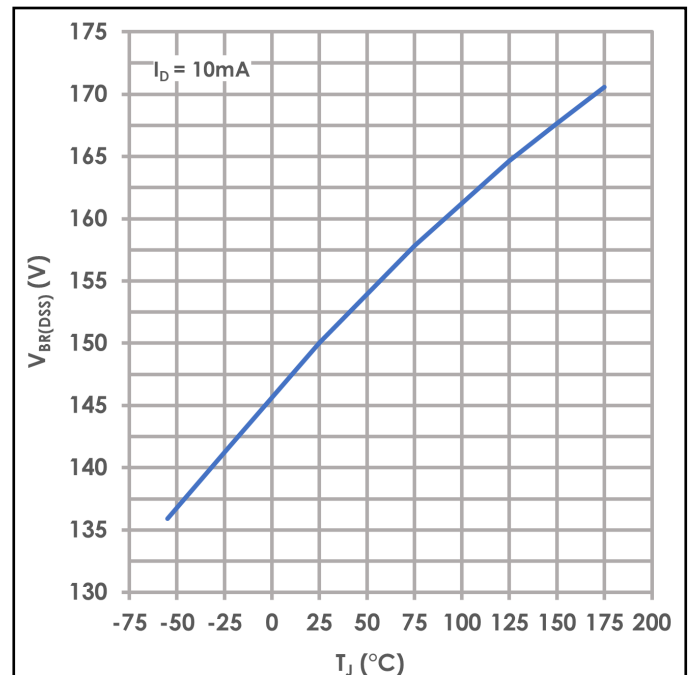


Figure 14: Min Drain-Source Breakdown Voltage

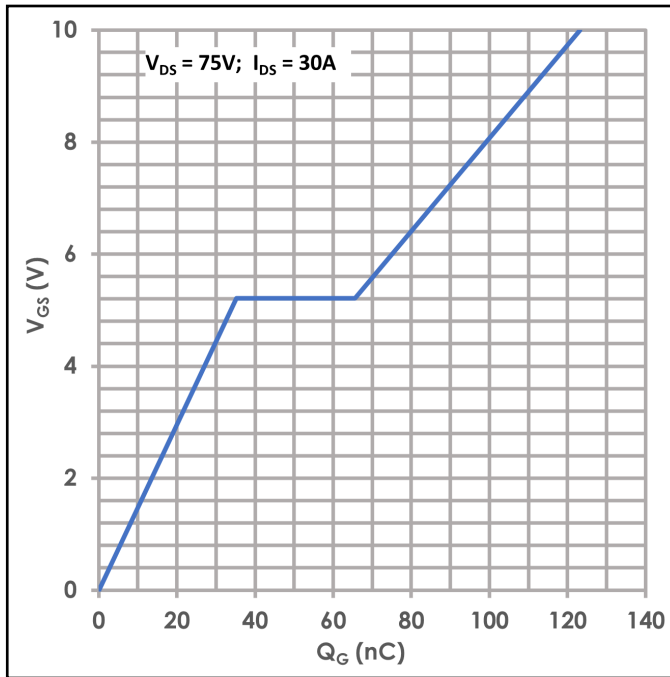


Figure 15: Typical Gate Charge

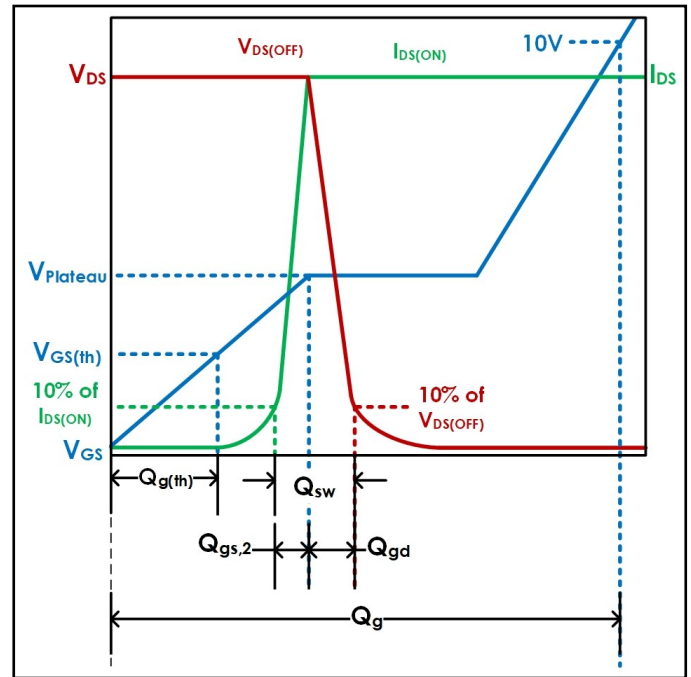
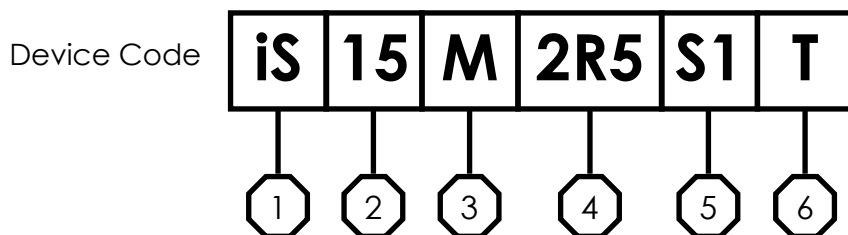








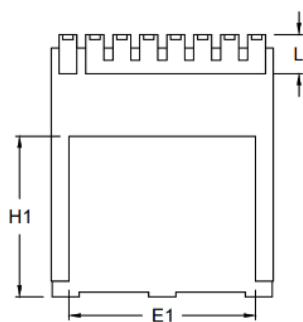
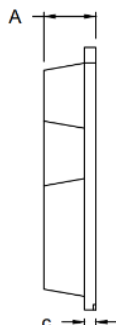
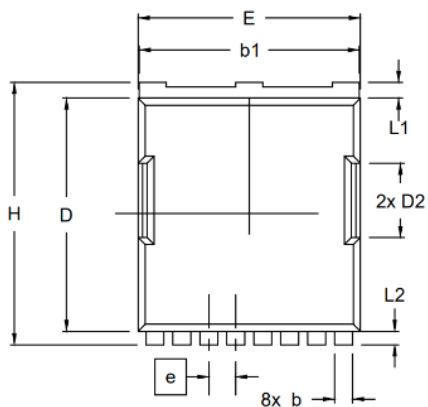
Figure 16: Gate Charge Definitions

DEVICE DECODER RING



-  1 - iDEAL Semiconductor product
-  2 - Voltage rating divided by 10 (150V)
-  3 - M = N-Channel MOSFET, Standard Threshold
-  4 - Maximum drain-to-source resistance
-  5 - SuperQ™ Generation
-  6 - T = TOLL

TOLL Package Drawing



SYMBOL	MIN	MAX
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
c	0.40	0.6
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.00
E1	7.90	8.60
e	1.20 BSC	
H	11.48	11.880
H1	6.75	7.43
L	1.40	2.10
L1	0.60	0.80
L2	0.500	0.700
θ	10° REF	

Notes:

1. All linear dimensions in millimeters



Revision History

Version	Date	Comments
1.0	February 2026	Initial Release



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