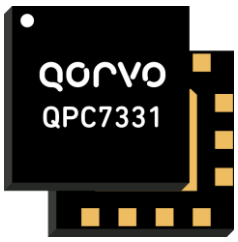
QPC7331

5MHz to 834MHz Variable Cable Slope Equalizer

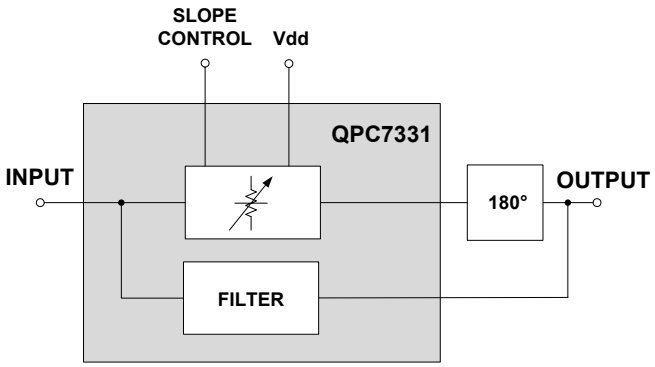
1. Product Overview and Benefits

The QPC7331 is a cable compensated voltage controlled variable equalizer employing SOI attenuator with operation bandwidth from 5MHz to 834MHz.



14 Pin 6 x 6 x 1.375 mm leadless SMT Package

2. Functional Block Diagram



Block Diagram

3. Key Features

- 5 – 834 MHz Operational Bandwidth
- Inverse cable loss frequency response
- 18dB slope range
- Low insertion loss
- High linearity
- 75Ohm impedance for CATV applications
- 5V single supply voltage
- Low power consumption

4. Applications

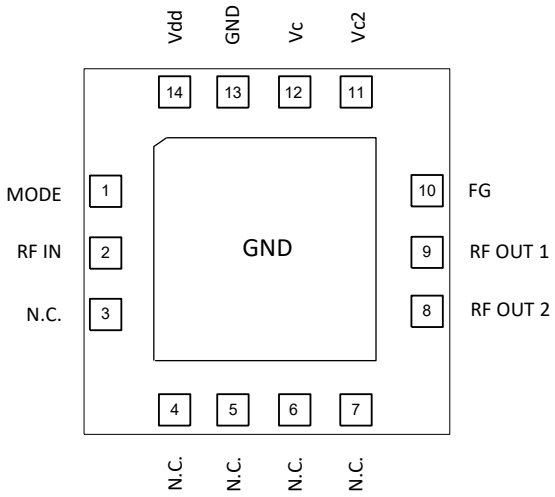
- CATV amplifier and transmission systems

5. Ordering Information

Part Number	Description
QPC7331SB	Sample bag 5 pcs
QPC7331SR	7” Reel with 100 pcs
QPC7331TR7	7” Reel with 500 pcs
QPC7331PCBA-410	Fully assembled Evaluation Board

6. Pin Configuration and Description

Top view



Pin Number	Label	Description
1	MODE	Slope control gradient (0V: positive slope control gradient or 5V: negative slope control gradient)
2	RF IN	RF input signal
8	RF OUT 2	Connection to balun and circuit output
9	RF OUT 1	Connection to balun
10	FG	Floating ground, connection to balun
11	Vc2	Control voltage 2
12	Vc	Control voltage
13	GND	Ground
14	Vdd	+5V supply voltage
3, 4, 5, 6, 7	N.C.	Not connected
Backside Pad	GND	Ground

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{DD})	-0.5 to +6V
Control Voltage (V_C)	-0.5 to +6V
Control Voltage 2 (V_{C2})	-2 to +24V
MODE	-0.5 to +6V
Storage Temperature	−40 to 100 °C

Operation of this device outside the parameter ranges given above may cause permanent damage.

7.2. Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Supply Voltage (V_{DD})		+5		V
Junction Temperature			+125	°C
Operating Mounting Base Temperature	-30		+100	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

7.3. Electrical Specifications

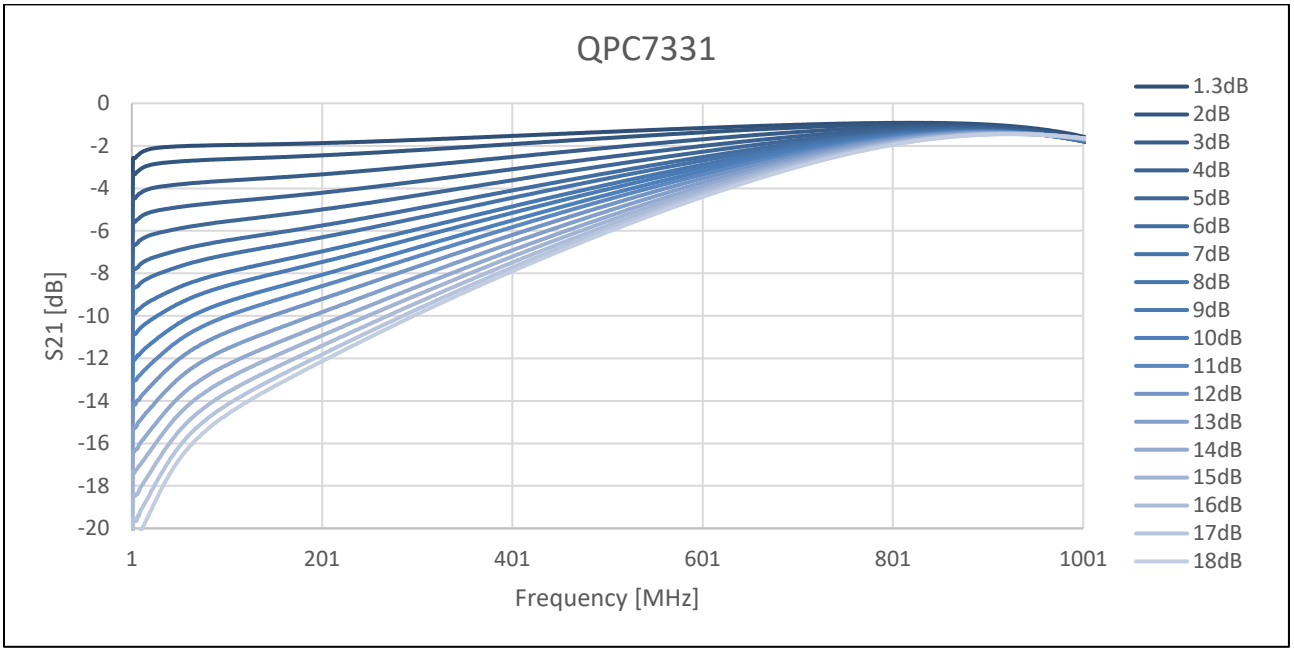
Parameter	Conditions (V_{DD}=5V, T_{MB}=25°C, Z_S=Z_L=75Ω)	Min.	Typ.	Max.	Units
Operational Frequency Range		5		834	MHz
Supply Current (I_{DD})			3		mA
RF Input Power	T ≤ +85°C			27	dBm
RF Input Power	+85°C < T ≤ +100°C			24	dBm
Input IP3	P_{IN} + ($IM3_{dBc}$/2) 6MHz tone spacing at 15dBm/tone	45	50		dBm
Input IP2	P_{IN} + $IM2_{dBc}$, IM2 is F1 + F2 6MHz tone spacing at 15dBm/tone		80		dBm
Minimum Slope [1]			1.3		dB
Maximum Slope [1]			18		dB
Insertion Loss (S21)	Slope set between 1dB and 15dB; f = 834MHz		1.7	2.5	dB
Flatness [2]	Slope set between 1dB and 15dB; f = 5 to 834MHz		0.6	1	dB
Input Return Loss (S11)	Slope set between 1dB and 18dB;		-18		dB
Output Return Loss (S22)	Slope set between 1dB and 18dB		-16		dB
Control Voltage (Vc) [3], positive slope control gradient	MODE = 0V, minimum slope at Vc = 0V	0	1 to 3	5	V
Control Voltage (Vc) [3], negative slope control gradient	MODE = 5V, minimum slope at Vc = 5V	0	2 to 4	5	V
Control Voltage 2 (Vc2) [3], positive slope control gradient	MODE = 0V, minimum slope at Vc2 = 0V	0	4 to 12	20	V
Control Voltage 2 (Vc2) [3], negative slope control gradient	MODE = 5V, minimum slope at Vc2 = 20V	0	8 to 16	20	V
MODE Pin Logic Low				0.4	V
MODE Pin Logic High		1			V

Notes:

1. Slope is defined as the difference between the gain at the start frequency and the gain at the stop frequency.
2. Flatness is defined as sum of positive and negative deviation from a straight line between gain at start frequency and gain at stop frequency.
3. Either Vc or Vc2 can be used to set slope, internal 1:4 voltage divider between Vc and Vc2.

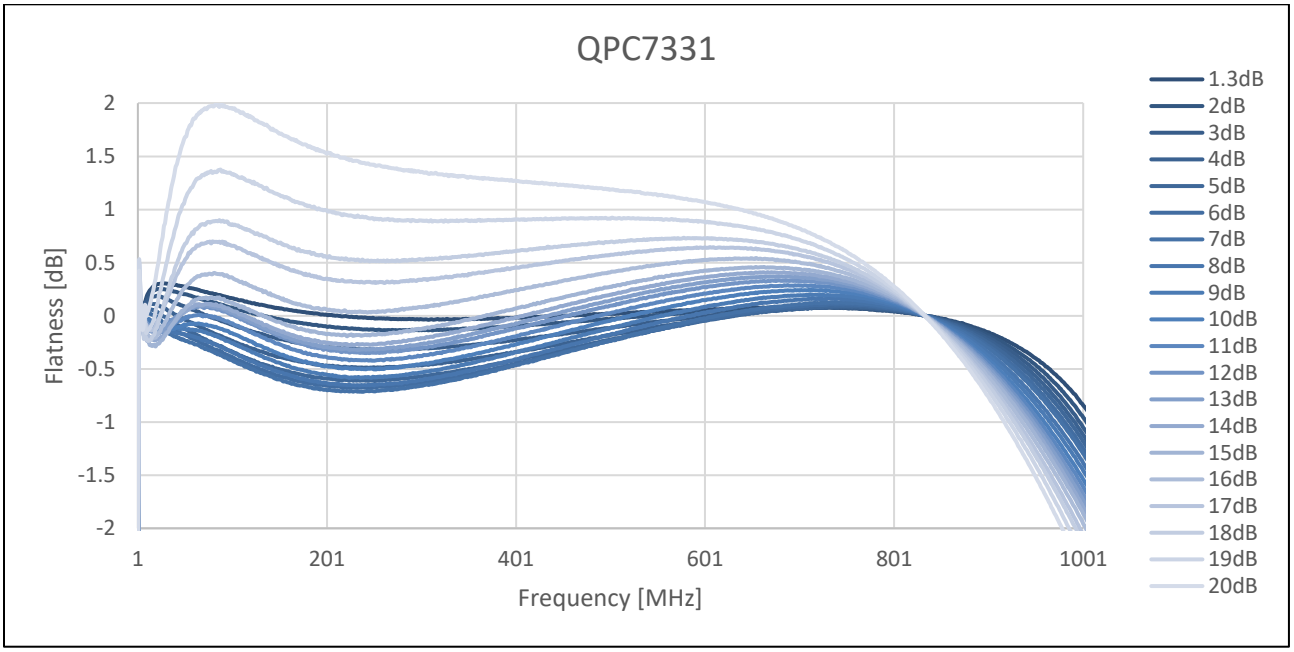
8. Slope vs Frequency

Test conditions unless otherwise noted: V_{DD} = +5.0 V, Temp. = +25 °C



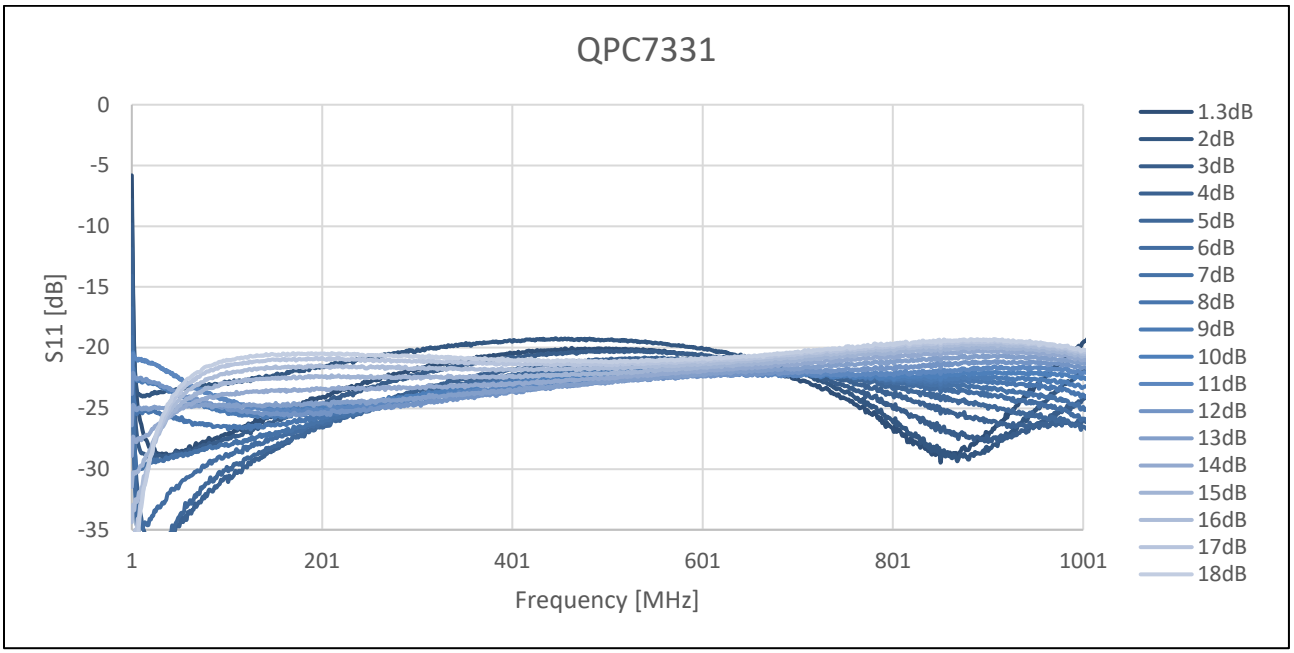
9. Flatness vs Slope

Test conditions unless otherwise noted: V_{DD} = +5.0 V, Temp. = +25 °C



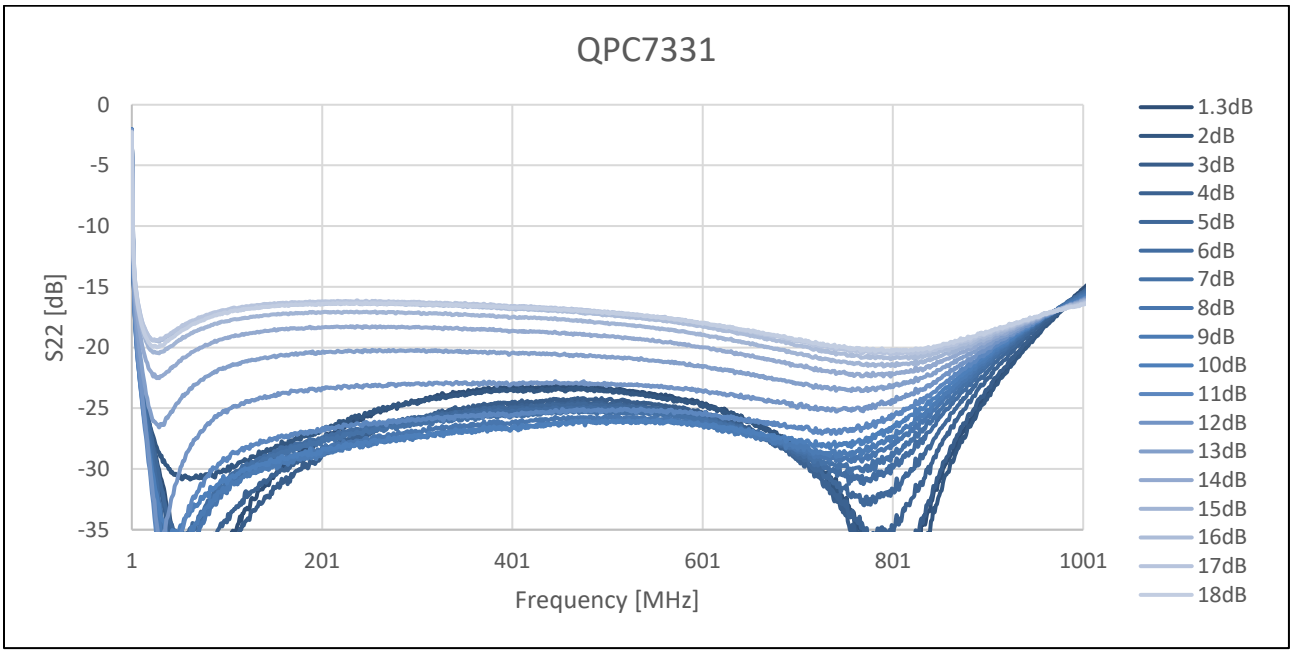
10. S_{11} vs Slope

Test conditions unless otherwise noted: V_{DD} = +5.0 V, Temp. = +25 °C

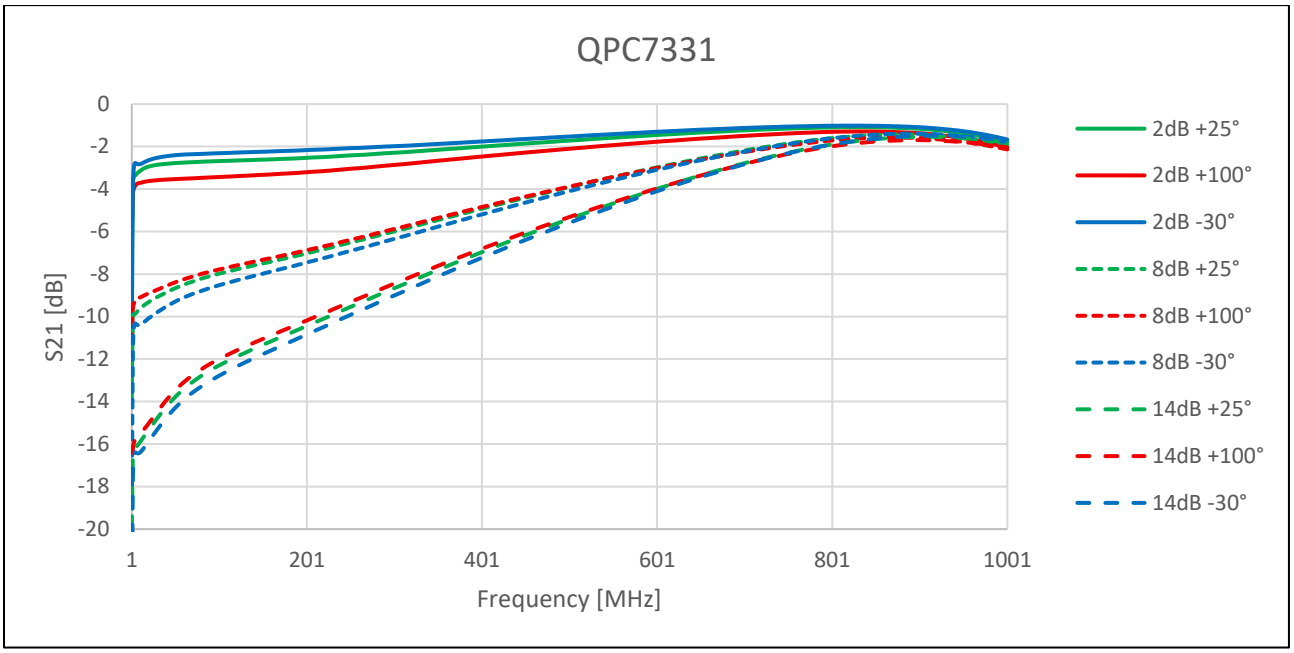


11. S_{22} vs Slope

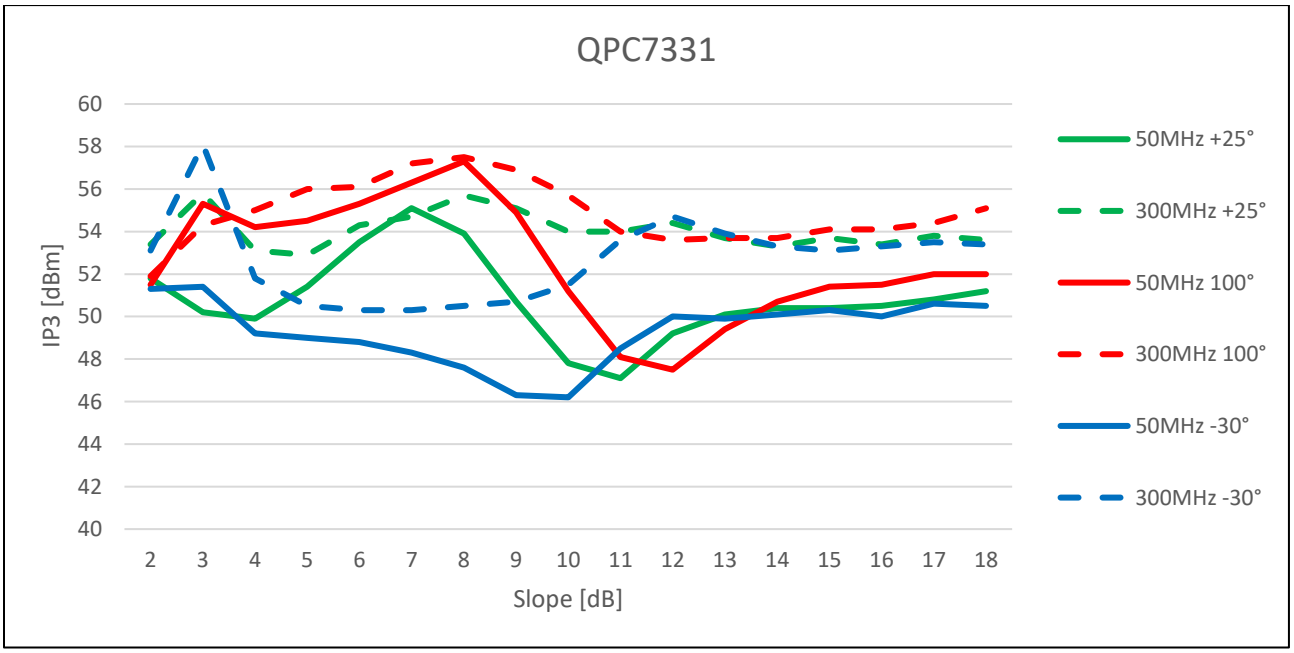
Test conditions unless otherwise noted: V_{DD} = +5.0 V, Temp. = +25 °C



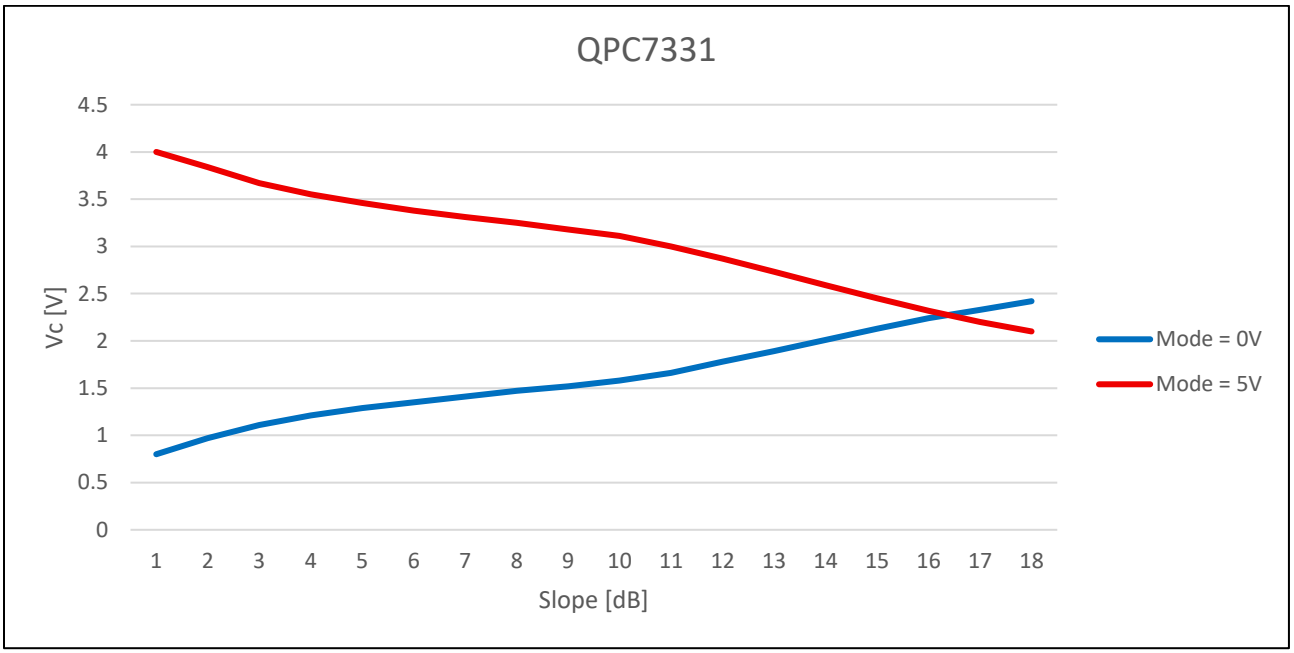
12. Slope vs. Temperature



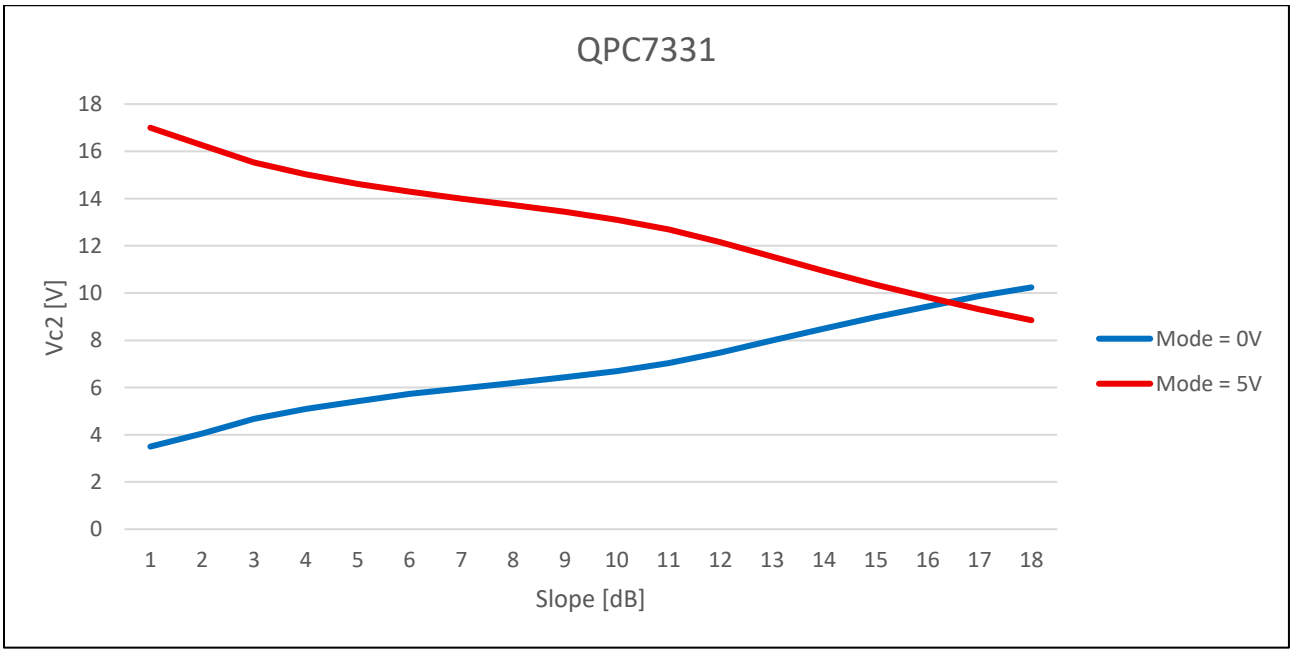
13. Input IP3 vs. Temperature



14. Slope vs Vc

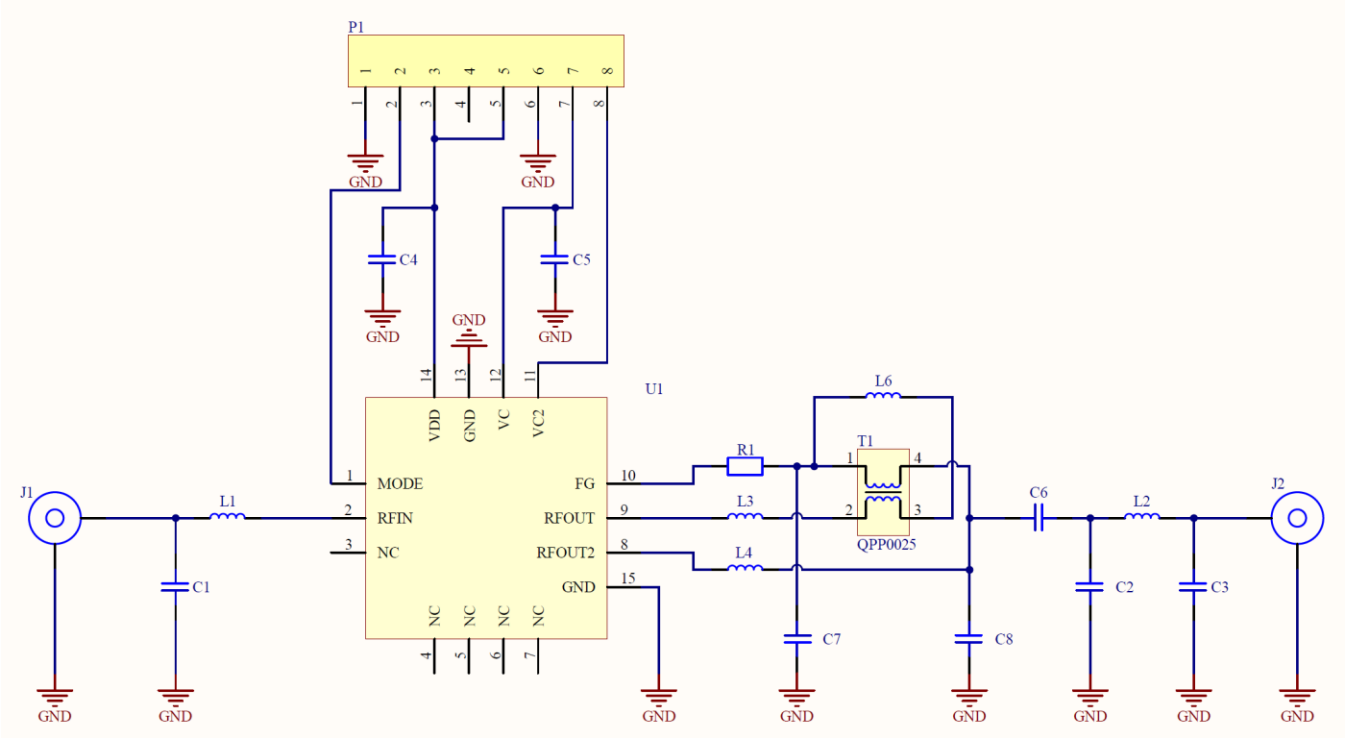


15. Slope vs Vc2



16. Application Information

16.1. Application Circuit Schematic

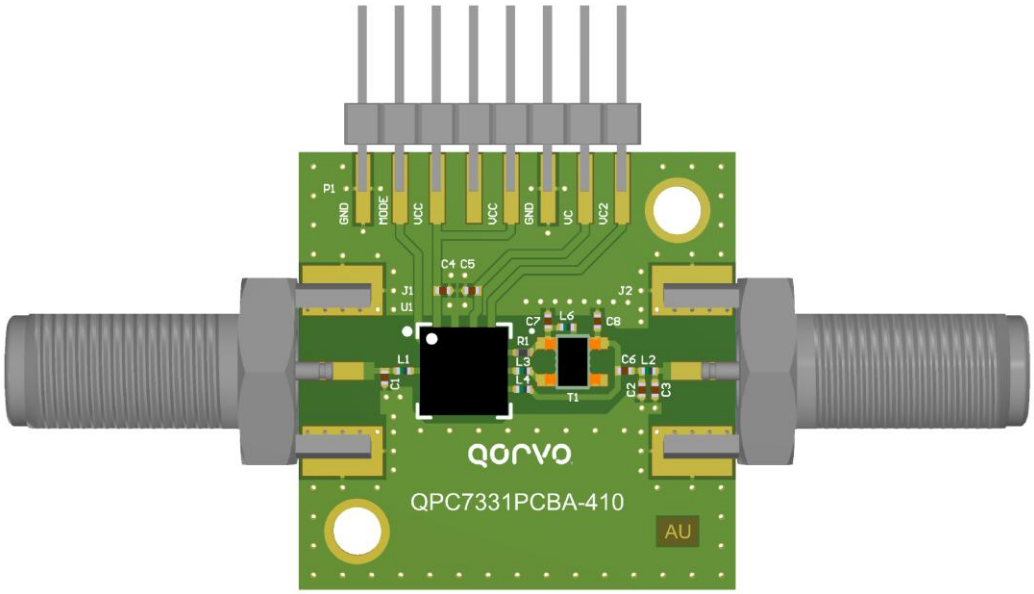


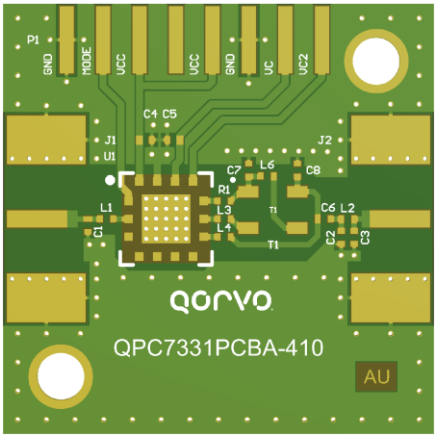
16.2. Bill of Material

Ref. Des.	Value	Description	Manuf.	Part Number
U1		Tilt MCM	Qorvo	QPC7331
C1	0.9 pF	Capacitor, Chip, 0402	Murata	
C3	0.5 pF	Capacitor, Chip, 0402	Murata	
C2, C7,C8	DNI	Capacitor, Chip, 0402	Murata	
C6	2.2 nF	Capacitor, Chip, 0402	Murata	
C4, C5	4.7 nF	Capacitor, Chip, 0402	Murata	
L1	6.2 nH	Inductor, Chip, 0402	Murata	LQP15HS6N2
L2	4.7 nH	Inductor, Chip, 0402	Murata	LQP15HS4N7
L3, L6	1 nH	Inductor, Chip, 0402	Murata	LQP15HS1N0
L4	1.8 nH	Inductor, Chip, 0402	Murata	LQP15HS1N8
R1	0 R	Resistor		
T1		Balun	Qorvo	QPP0025
J1, J2		Connector F-type, female	Amphenol	222181
P1		Connector, 2.54mm pin spacing, optional		

Notes: C1, L1, C2, C3, L2 may be modified in target application circuit for S11 and S22 optimization

16.3. Evaluation Board Assembly Drawing





Evaluation board PCB: FR4, double sided, 1.5mm thickness, 35um Cu

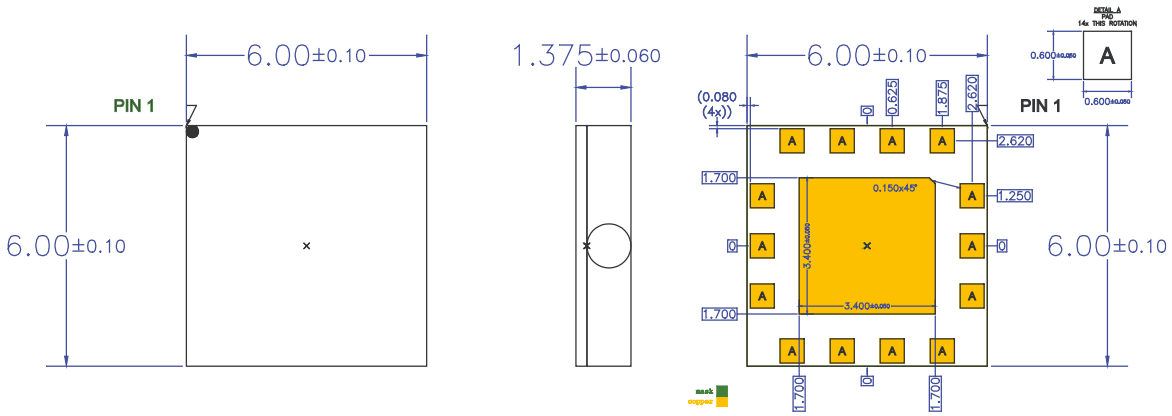
The ground plane of the QPC7331 module should be soldered onto a board equipped with thermal vias. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.010”).

Gerber Files available on request

17. Packaging and Ordering Information

17.1. Device Marking and Package Dimensions

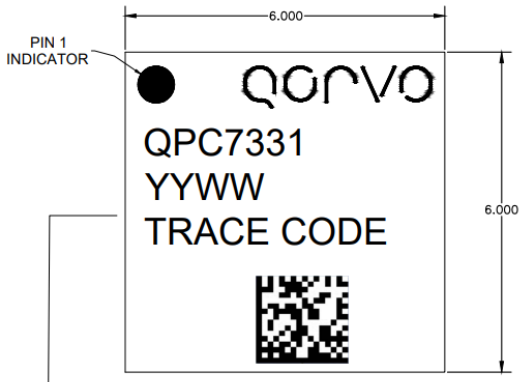
Marking: Part number – QPC7331



TOP VIEW SIDE VIEW BOTTOM VIEW

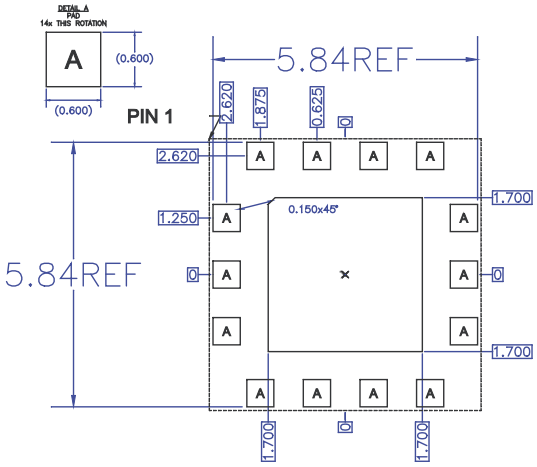
Notes:
1. All dimensions are in microns. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

17.2. Marking Diagramm

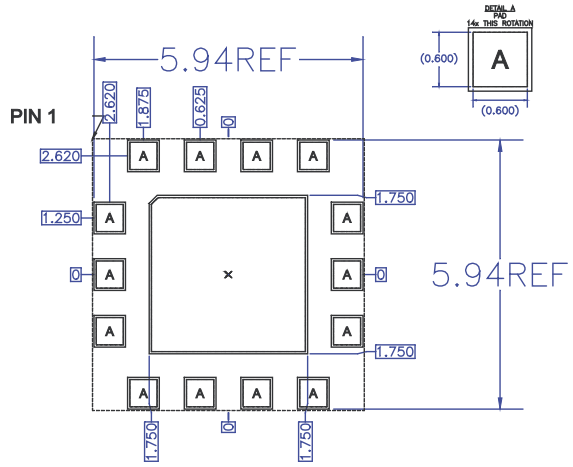


PIN 1 INDICATOR
LOGO: USE Qo1T LOGO
LINE 1: QPC7331
LINE 2: PRODUCTION DATA CODE YYWW
YY = LAST TWO DIGITS OF THE CALENDAR YEAR
WW = WEEK NUMBER OF ASSEMBLY
LINE 3: TRACE CODE REFER TO P.O. FOR TRACE CODE
LAST LINE: 2DID BARCODE

17.3. PCB Footprint Recommendations



RECOMMENDED
LAND PATTERN



RECOMMENDED
LAND PATTERN MASK

All dimensions are in millimeters. Angles are in degrees.

18. Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	2	ESDA/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

19. Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: ENEPIG (NiPdAu)

20. Environmental Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- SVHC Free
- PFOS Free

21. Revision History

Revision	Description
B	Initial product release