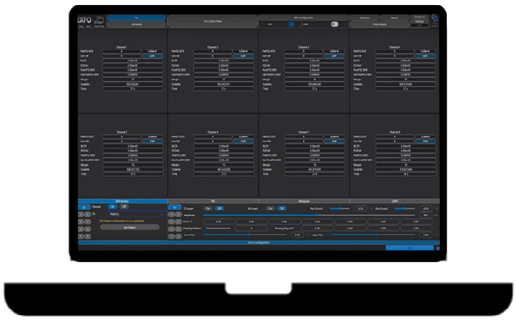
SPEC SHEET

BA-1600-OSFP

1.6T DUAL-PORT BIT ANALYZER



- Achieve up to 3.2T testing capacity with two independent 1.6T OSFP ports. Test solution optimized for cable and transceiver validation.

KEY FEATURES

Test two 1.6T transceivers or an end-to-end high-speed interconnect using the dual OSFP ports

Full lifecycle validation for 1.6T, 800G and 400G across lab, fab and live environments

Superior hardware design: native OSFP interfaces, excellent signal quality, clean eye diagram and low error floor

Real-time FEC generation and analysis: testing of pre/post FEC BER, symbol error distribution and FEC margin

BLER: Block error ratio statistics and an efficient FLR estimation mechanism, addressing the time constraints of ultra-low BER measurements

PAM4 support for validating high-speed signaling performance

High-performance signal integrity and BER testing for validating compliance and performance in next-gen 1.6T transceivers and cables

User-friendly GUI streamlines workflows, and reduces learning curves

Powerful equalizer and channel simulator: powerful equalizer includes CTLE

I²C register read/write access enables the direct control and monitoring of device parameters for fast, low-level diagnostics and efficient debugging

“Save-and-load” functionality for all applicable parameters reduces valuable time and ensures test consistency

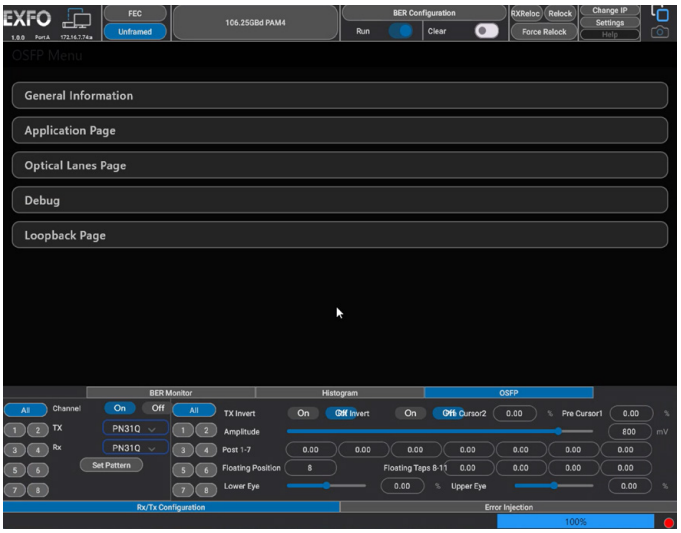
Automation simplifies complex test configurations and speeds up validation using a complete API suite

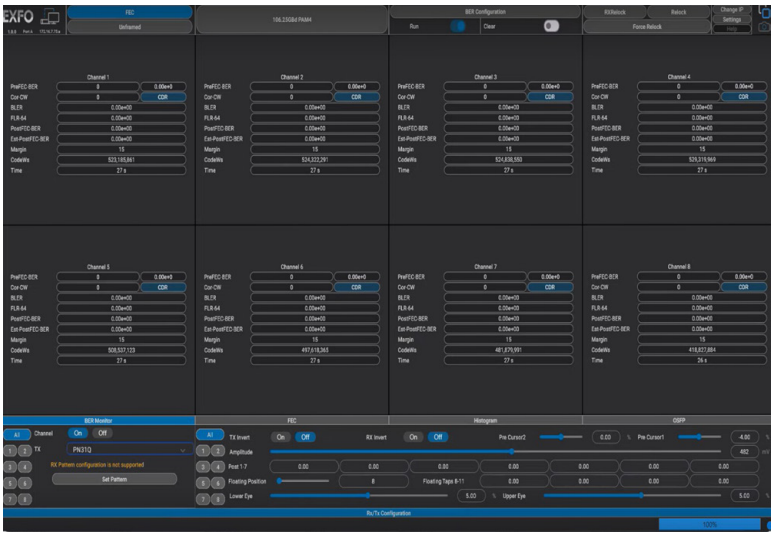
I2C Target 3-pin connector that allows for external control of the OSFP

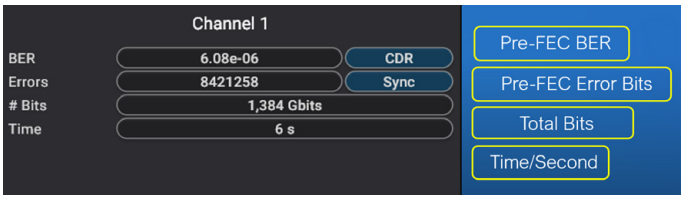
ES France - Département Tests & Mesures
127 rue de Buzenval BP 26 - 92380 Garches
Tél. 01 47 95 99 45
e-mail : tem@es-france.com
Site Web : www.es-france.com

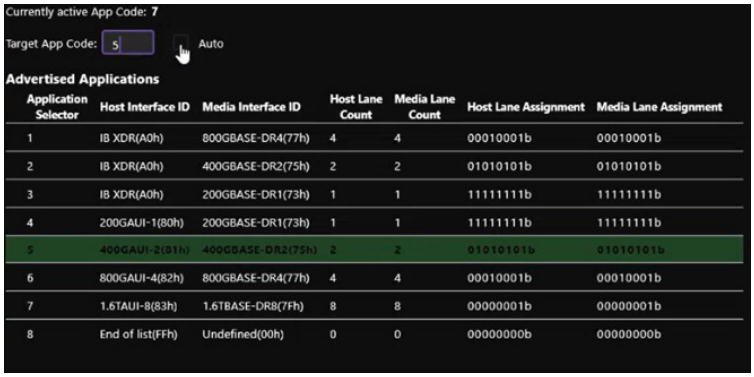
POWERFUL AND SIMPLIFIED USER INTERFACE

The BA-1600 graphical user interface (GUI) provides simplified and real-time test results per channel. It requires an external Windows-based PC with Ethernet capability to run the GUI and API.

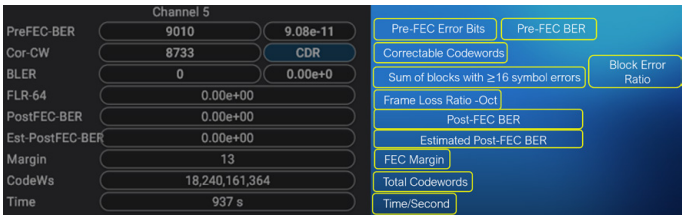








Application Selector	Host Interface ID	Media Interface ID	Host Lane Count	Media Lane Count	Host Lane Assignment	Media Lane Assignment
1	IB XDR(A0h)	800GBASE-DR4(77h)	4	4	00010001b	00010001b
2	IB XDR(A0h)	400GBASE-DR2(75h)	2	2	01010101b	01010101b
3	IB XDR(A0h)	200GBASE-DR1(73h)	1	1	11111111b	11111111b
4	200GAUI-1(80h)	200GBASE-DR1(73h)	1	1	11111111b	11111111b
5	400GAUI-2(81h)	400GBASE-DR2(75h)	2	2	01010101b	01010101b
6	800GAUI-4(82h)	800GBASE-DR4(77h)	4	4	00010001b	00010001b
7	1.6TAUI-8(83h)	1.6TBASE-DR8(7Fh)	8	8	00000001b	00000001b
8	End of list(FFh)	Undefined(00h)	0	0	00000000b	00000000b



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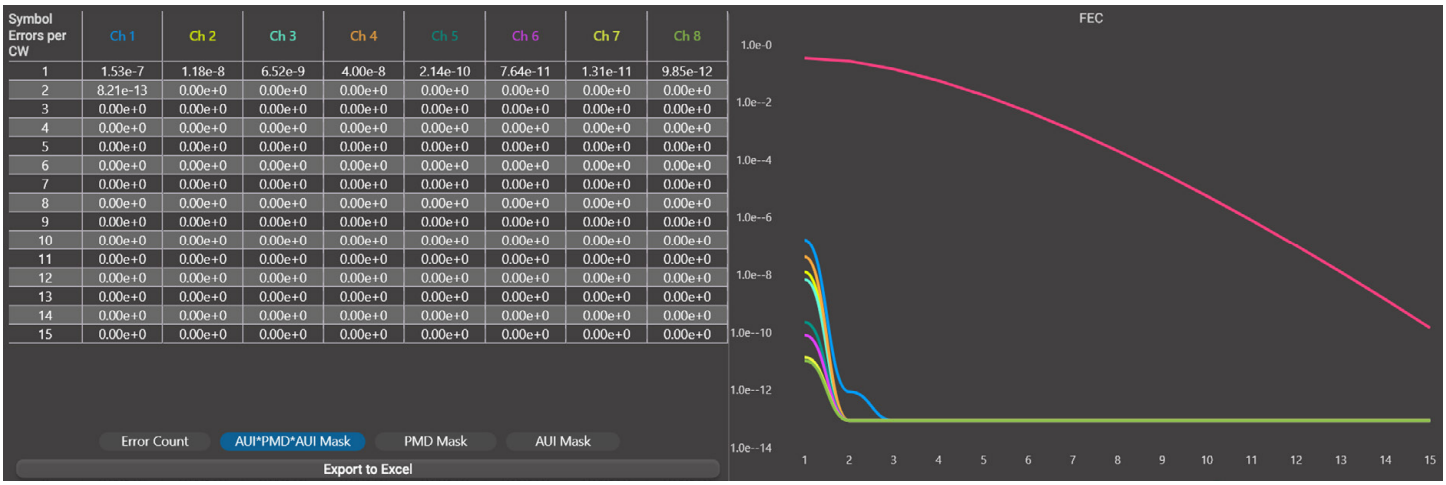
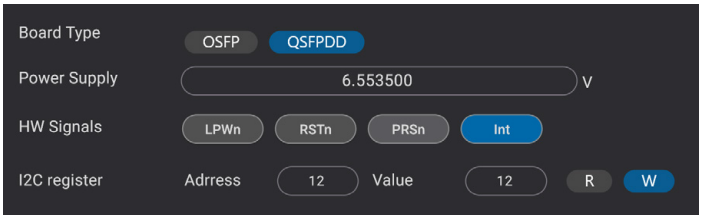
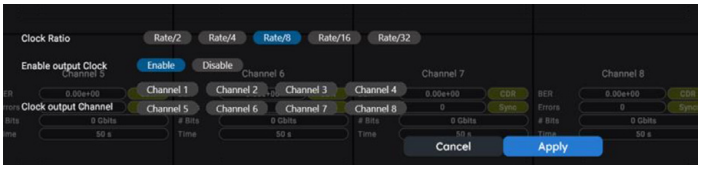


FEC channel distribution and BLER mask testing

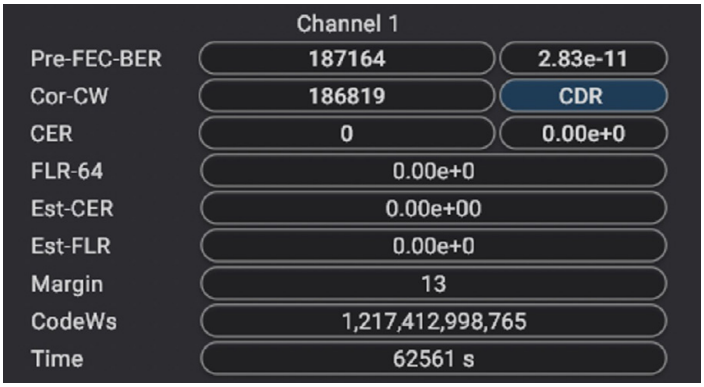


MCB control



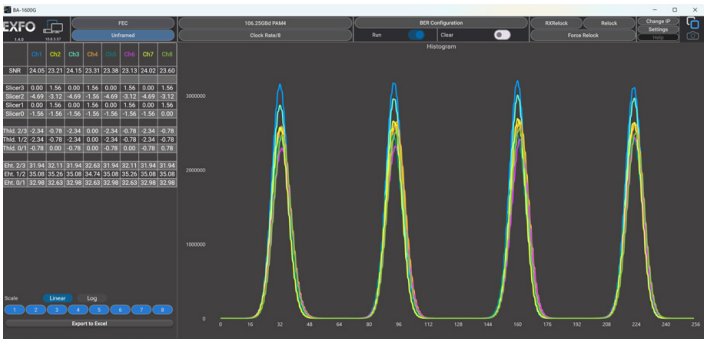
Reference clock

WITH PAM4 CODING, A SIMPLE BER TEST IS NOT ENOUGH



FEC symbol error margin

FEC symbol error distribution plot

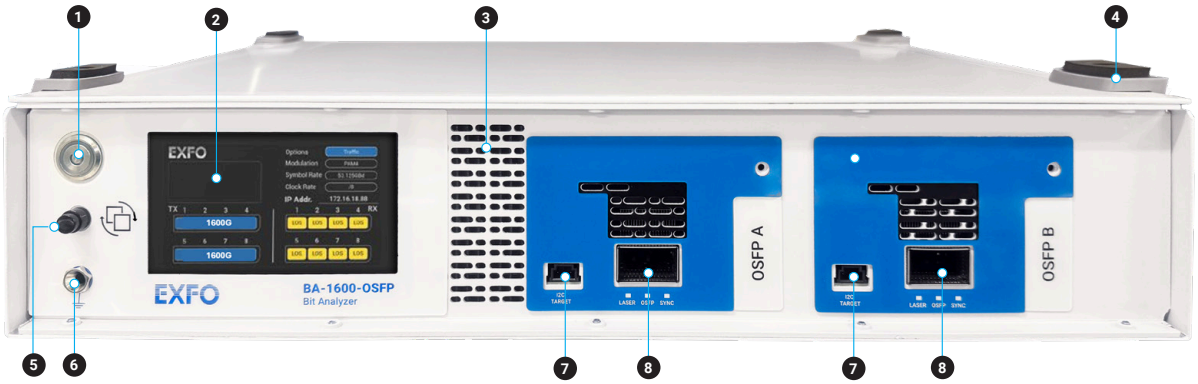


Channel histogram

14-tap mode

DESIGNED FOR HIGH-SPEED AND MULTISERVICE

1. Power button
2. Display (4.5 inch)
3. Air inlet
4. Foot rest
5. Screen switch button
6. Grounding jack
7. I2C Target 3-pin connector
8. OSFP cage



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SPECIFICATIONS

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Number of ports	2
Data rate per lane (GBd)	106.25, 53.125 and 26.5625
Data rate adjustment (ppm)	±250
PAM4 coding	Gray code
Pattern supported by PPG and ED	PPG: PRBS 7Q/9Q/10Q/11Q/13Q/15Q/20Q/23Q/31Q/49Q/58Q/SSPRQ/SQUARE_WAVE ED: PRBS 7Q/9Q/10Q/11Q/13Q/15Q/20Q/23Q/31Q/49Q/58Q [a]
PG maximum amplitude (mV_{ppd})	900
Jitter RMS (mUI)	≤23
EOJ03 (mUI)	≤25
JH4u (mUI)	≤135
ED maximum level (mV_{ppd})	1200
ED damage level (mV_{ppd})	1300
TX multi tap pre-emphasis support	10 fix taps + 4 floating taps [b]
Connector type	OSFP IHS

GENERAL SPECIFICATIONS		
Size (H × W × D)		105 mm × 465 mm × 350 mm (4.1 in × 18.3 in × 13.8 in)
Weight		≤ 5 kg (11 lb)
Temperature	Operating Storage	0 °C to 40 °C (32 °F to 104 °F) −40 °C to 70 °C (-40 °F to 158 °F)
Relative humidity		≤95% non-condensing
Power		100 Vac to 240 Vac (47 Hz to 63 Hz) 200W typical / 300W max

ACCESSORIE	
GP-3277	19” relay rack mounting bracket + screws/HW

a. Only 13Q, 20Q, 23Q, 31Q, 49Q, 58Q patterns are supported in RX at 106.25 GBaud.

b. Max 14 UI away from fix taps.