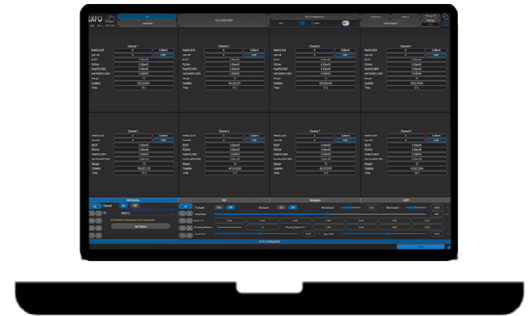


BA-1600-OSFP

1.6T DUAL-PORT BIT ANALYZER

- Achieve up to 3.2T testing capacity with two independent 1.6T OSFP ports. Test solution optimized for cable and transceiver validation.



KEY FEATURES

Test two 1.6T transceivers or an end-to-end high-speed interconnect using the dual OSFP ports

Full lifecycle validation for 1.6T, 800G and 400G across lab, fab and live environments

Superior hardware design: native OSFP interfaces, excellent signal quality, clean eye diagram and low error floor

Real-time FEC generation and analysis: testing of pre/post FEC BER, symbol error distribution and FEC margin

BLER: Block error ratio statistics and an efficient FLR estimation mechanism, addressing the time constraints of ultra-low BER measurements

PAM4 support for validating high-speed signaling performance

High-performance signal integrity and BER testing for validating compliance and performance in next-gen 1.6T transceivers and cables

User-friendly GUI streamlines workflows, and reduces learning curves

Powerful equalizer and channel simulator: powerful equalizer includes CTLE

I²C register read/write access enables the direct control and monitoring of device parameters for fast, low-level diagnostics and efficient debugging

“Save-and-load” functionality for all applicable parameters reduces valuable time and ensures test consistency

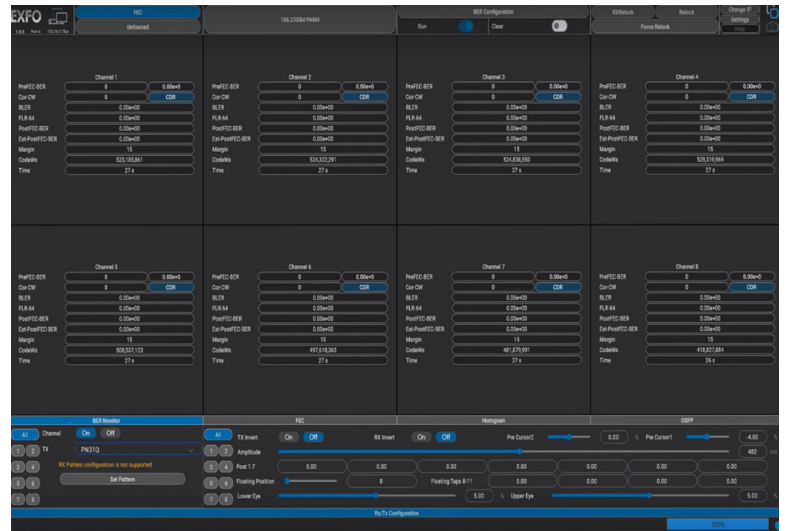
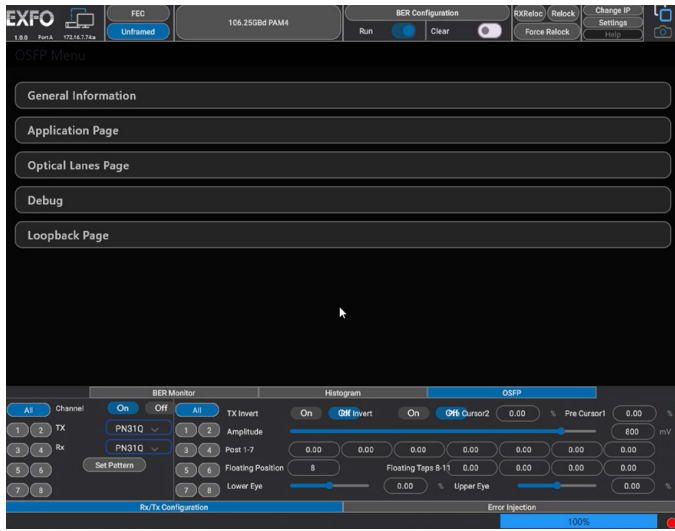
Automation simplifies complex test configurations and speeds up validation using a complete API suite

I²C Target 3-pin connector that allows for external control of the OSFP



POWERFUL AND SIMPLIFIED USER INTERFACE

The BA-1600 graphical user interface (GUI) provides simplified and real-time test results per channel. It requires an external Windows-based PC with Ethernet capability to run the GUI and API.



General Information		Module Specifics	
Module ID	OSFP	Current	Max
Module Name	1600	0.00e+00	0.00e+00
Serial Number	1600	3.37e-01	3.30e-01
Local Number	1600	2.92e-01	2.92e-01
Host Position	16	0.00e+00	0.00e+00
Module Temp	16	0.00e+00	0.00e+00

Channel 1

BER: **6.08e-06** CDR

Errors: **8421258** Sync

Bits: **1,384 Gbits**

Time: **6 s**

Pre-FEC BER
 Pre-FEC Error Bits
 Total Bits
 Time/Second

Currently active App Code: 7

Target App Code: Auto

Application Selector	Host Interface ID	Media Interface ID	Host Lane Count	Media Lane Count	Host Lane Assignment	Media Lane Assignment
1	IB XDR(A0h)	800GBASE-DR4(77h)	4	4	00010001b	00010001b
2	IB XDR(A0h)	400GBASE-DR2(75h)	2	2	01010101b	01010101b
3	IB XDR(A0h)	200GBASE-DR1(73h)	1	1	11111111b	11111111b
4	200GAUI-1(80h)	200GBASE-DR1(73h)	1	1	11111111b	11111111b
5	400GAUI-2(91h)	400GBASE-DR2(75h)	2	2	01010101b	01010101b
6	800GAUI-4(82h)	800GBASE-DR4(77h)	4	4	00010001b	00010001b
7	1.6TAUI-8(83h)	1.6TBASE-DR8(7Fh)	8	8	00000001b	00000001b
8	End of list(FFh)	Undefined(00h)	0	0	00000000b	00000000b

Channel 5

PreFEC BER: **9010** 9.08e-11

Cor-CW: **8733** CDR

BLER: **0** 0.00e+0

FLR-64: **0.00e+00**

PostFEC BER: **0.00e+00**

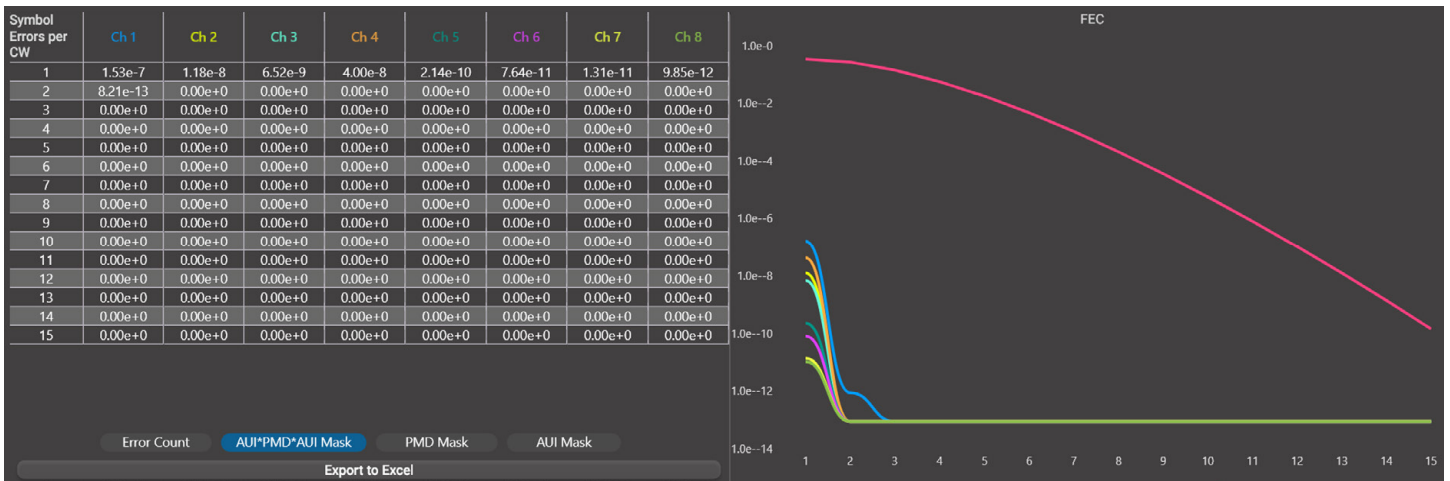
Est-PostFEC BER: **0.00e+00**

Margin: **13**

CodeWs: **18,240,161,364**

Time: **937 s**

Pre-FEC Error Bits
 Pre-FEC BER
 Correctable Codewords
 Sum of blocks with ≥ 16 symbol errors
 Block Error Ratio
 Frame Loss Ratio-Oct
 Post-FEC BER
 Estimated Post-FEC BER
 FEC Margin
 Total Codewords
 Time/Second



FEC channel distribution and BLER mask testing

Board Type: OSFP, **QSFPDD**

Power Supply: 6.553500 V

HW Signals: LPWn, RSTn, PRSh, **Int**

I2C register: Address 12, Value 12, R, **W**

MCB control

Clock Ratio: Rate/2, Rate/4, **Rate/8**, Rate/16, Rate/32

Enable output Clock: Channel 3 **Enable**, Channel 6 **Disable**

Clock output Channel: Channel 1, Channel 2, Channel 3, Channel 4, Channel 5, Channel 6, Channel 7, Channel 8

Buttons: Cancel, **Apply**

Reference clock

WITH PAM4 CODING, A SIMPLE BER TEST IS NOT ENOUGH

Channel 1

Pre-FEC-BER: 187164, 2.83e-11

Cor-CW: 186819, CDR

CER: 0, 0.00e+0

FLR-64: 0.00e+0

Est-CER: 0.00e+00

Est-FLR: 0.00e+0

Margin: 13

CodeWws: 1,217,412,998,765

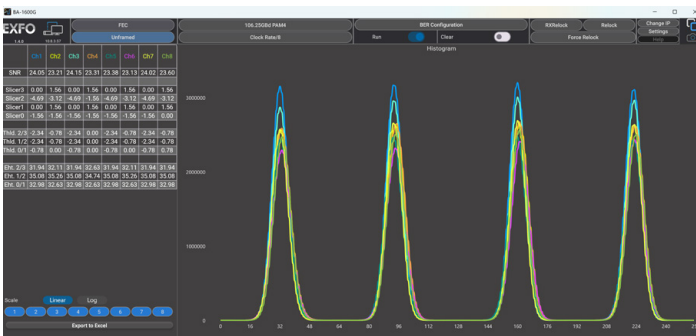
Time: 62561 s

FEC symbol error margin

EXFO 106.25Gb/s PAM4

Number of Symbols	Ch 1	Ch 2	Ch 3	Ch 4	Ch 5	Ch 6	Ch 7	Ch 8
1	0	111	8	32	1	0	0	0
2	0	18	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0

FEC symbol error distribution plot



Channel histogram

14-tap mode

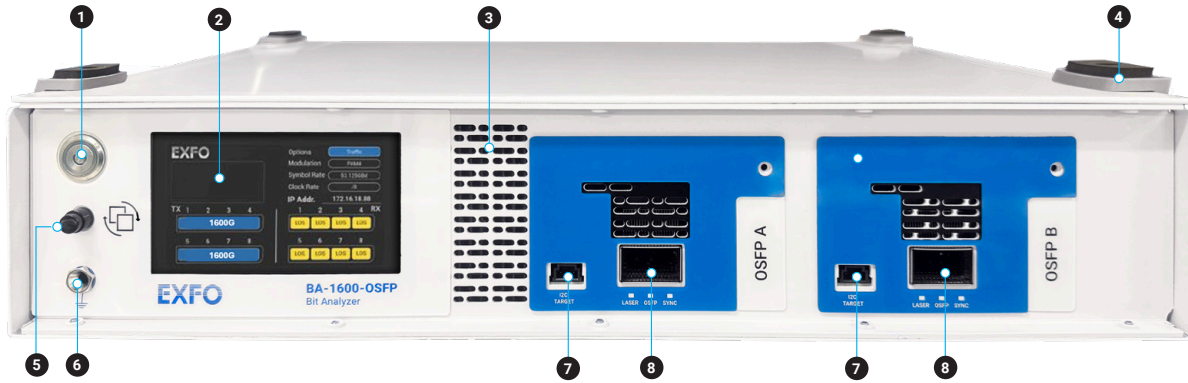
Buttons: TX Invert, RX Invert, Pre Cursor2, Pre Cursor1, Amplitude, Post 1-7, Lower Eye, Upper Eye

14-tap mode



DESIGNED FOR HIGH-SPEED AND MULTISERVICE

- 1 Power button
- 2 Display (4.5 inch)
- 3 Air inlet
- 4 Foot rest
- 5 Screen switch button
- 6 Grounding jack
- 7 I2C Target 3-pin connector
- 8 OSFP cage



SPECIFICATIONS

SPECIFICATIONS	
Number of ports	2
Data rate per lane (GBd)	106.25, 53.125 and 26.5625
Data rate adjustment (ppm)	±250
PAM4 coding	Gray code
Pattern supported by PPG and ED	PPG: PRBS 7Q/9Q/10Q/11Q/13Q/15Q/20Q/23Q/31Q/49Q/58Q/SSPRQ/SQUARE_WAVE ED: PRBS 7Q/9Q/10Q/11Q/13Q/15Q/20Q/23Q/31Q/49Q/58Q ^a
PG maximum amplitude (mV _{ppd})	900
Jitter RMS (mUI)	≤23
EOJ03 (mUI)	≤25
JH4u (mUI)	≤135
ED maximum level (mV _{ppd})	1200
ED damage level (mV _{ppd})	1300
TX multi tap pre-emphasis support	10 fix taps + 4 floating taps ^b
Connector type	OSFP IHS

GENERAL SPECIFICATIONS	
Size (H × W × D)	105 mm × 465 mm × 350 mm (4.1 in × 18.3 in × 13.8 in)
Weight	≤ 5 kg (11 lb)
Temperature	Operating: 0 °C to 40 °C (32 °F to 104 °F) Storage: -40 °C to 70 °C (-40 °F to 158 °F)
Relative humidity	≤95% non-condensing
Power	100 Vac to 240 Vac (47 Hz to 63 Hz) 200W typical / 300W max

ACCESSORIE	
GP-3277	19" relay rack mounting bracket + screws/HW

a. Only 13Q, 20Q, 23Q, 31Q, 49Q, 58Q patterns are supported in RX at 106.25 GBaud.

b. Max 14 UI away from fix taps.