

SuperQ™ 200-V N-Channel Power MOSFET

FEATURES

- 175°C Industrial temperature rating
- Robustness under fault conditions
- 100% UIS tested in production
- Low switching losses, Q_{sw} and E_{oss}
- Easier paralleling with $\pm 0.5V$ gate threshold

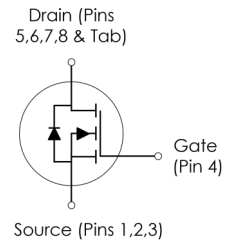
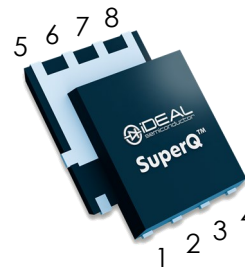
APPLICATIONS

- Motor control
- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier

DESCRIPTION

Engineered for SMPS and high-efficiency motor drives, this 200V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust PDFN 5x6mm package. Featuring best-in-class $R_{DS(on)}$ and Q_{sw} , it minimizes heat dissipation at both full and partial loads.

PRODUCT SUMMARY



PDFN 5x6mm

Parameter	Value	Unit
$T_A = 25^\circ C$		
V_{DS}	200	V
$R_{DS(on),max}$	25	m Ω
I_D	45	A
Q_G	27.5	nC
Q_{sw}	2.5	nC
E_{oss}	1	μJ



ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS20M028S1C	PDFN5x6	iS20M028S1	13" 5,000pcs T&R

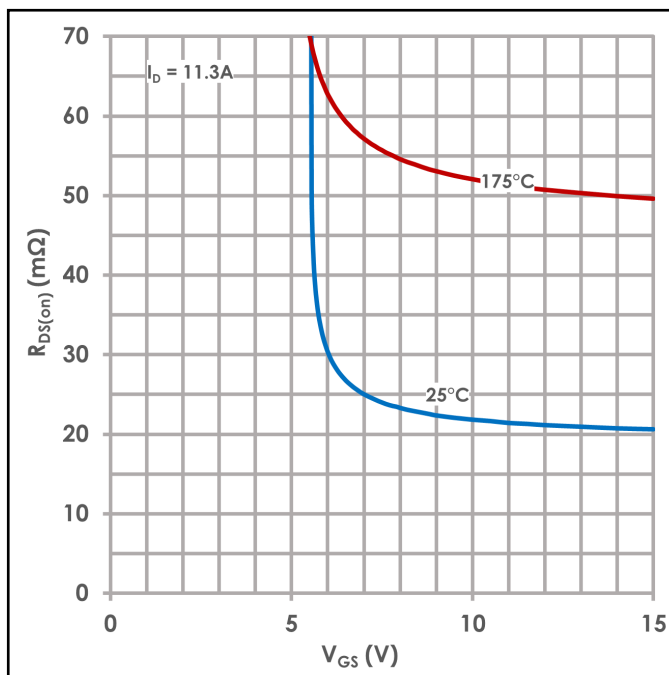


Figure 1: Typical Drain-Source On Resistance

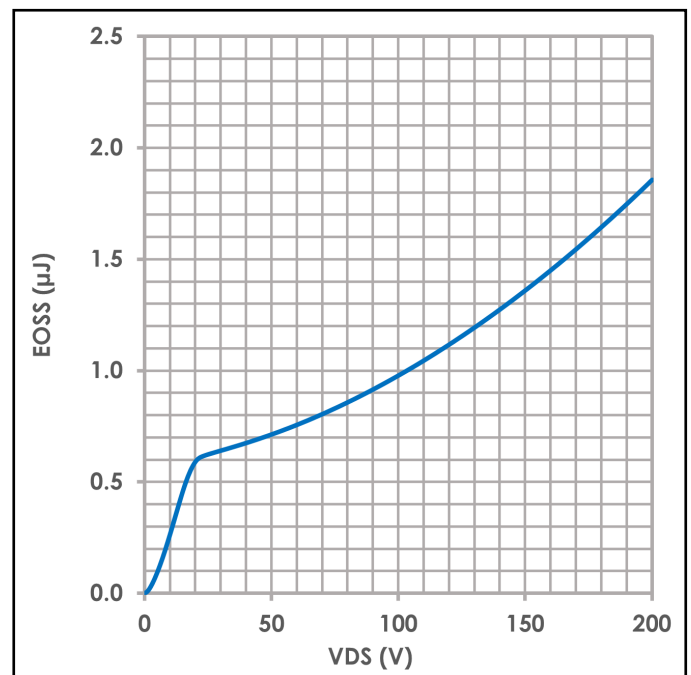


Figure 2: Typical COSS Stored Energy



ABSOLUTE MAXIMUM RATINGS			
SYMBOL	PARAMETER (T _A = 25°C unless otherwise specified)	VALUE	UNIT
V _{GS}	Gate-to-source voltage	± 20	V
I _D	Continuous drain current (silicon limited), T _C = 25°C	45	A
	Continuous drain current (silicon limited), T _C = 100°C	32	
I _{DM}	Pulsed drain current	162	A
P _D	Power dissipation, T _C = 25°C	125	W
T _J , T _{STG}	Operating junction, storage temperature	-55 to 175	°C
E _{AS}	Avalanche energy, single pulse I _D = 18.3A, R _{GS} = 25Ω	168	mJ

THERMAL CHARACTERISTICS					
SYMBOL	PARAMETER (T _A = 25°C unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
R _{θJC}	Junction-to-case thermal resistance - PDFN 5x6mm	-	-	1.2	°C/W
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	-	-	50	°C/W

(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.



ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	$V_{GS} = 0V, I_D = 1mA$	200	-	-	V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0V, V_{DS} = 160V, T_J = 25^\circ\text{C}$	-	0.03	1	μA
		$V_{GS} = 0V, V_{DS} = 160V, T_J = 125^\circ\text{C}^{(2)}$	-	12	100	
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0V, V_{GS} = 20V$	-	1	100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 70\mu\text{A}$	3.1	3.6	4.1	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 10V, I_D = 11.3A$	-	22	25	m Ω
g_{fs}	Transconductance	$V_{DS} = 10V, I_D = 11.3A$	14	28	-	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance ⁽²⁾	$V_{GS} = 0V, V_{DS} = 100V, f = 100\text{kHz}$	-	1,886	2,451	pF
C_{rss}	Reverse transfer capacitance ⁽²⁾		-	12	16	
C_{oss}	Output capacitance ⁽²⁾		-	65	85	
$C_{o(er)}$	Effective output capacitance	$V_{DS} = 0 \text{ to } 100V, V_{GS} = 0V$	-	197	-	
R_G	Series gate resistance	$f = 1\text{MHz}$	-	3.1	4.7	Ω
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 100V, V_{GS} = 10V, I_{DS} = 11.3A,$ $R_{G,EXT} = 0\Omega$	-	9.3	-	ns
t_r	Rise time		-	2	-	
$t_{d(off)}$	Turn-off delay time		-	28	-	
t_f	Fall time		-	12.7	-	
GATE CHARGE CHARACTERISTICS						
Q_G	Gate charge total ⁽²⁾	$V_{DS} = 100V, I_D = 11.3A,$ $V_{GS} = 0 \text{ to } 10V$	-	27.5	36	nC
Q_{sw}	Switching charge ⁽³⁾		-	2.5	-	
Q_{gd}	Gate to drain charge ^{(2) (3)}		-	1.2	1.6	
$Q_{g(th)}$	Gate charge at threshold		-	6.7	-	
$V_{plateau}$	Gate plateau voltage		-	5.5	-	V
Q_{oss}	Output charge ⁽²⁾	$V_{DS} = 0 \text{ to } 100V, V_{GS} = 0V$	-	95	109	nC
E_{oss}	Capacitive stored energy		-	1	-	μJ
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_{SD} = 11.3A, V_{GS} = 0V$	-	1	1.2	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 100V, I_F = 11.3A,$	-	440	-	nC
t_{rr}	Reverse recovery time	$di/dt = 100A/\mu\text{s}$	-	108	-	ns

(2) Defined by design. Not subject to production test.

(3) Q_{sw} should be used for switching loss calculations. See Q_{sw} application note on www.idealsemi.com. See Figure 16.

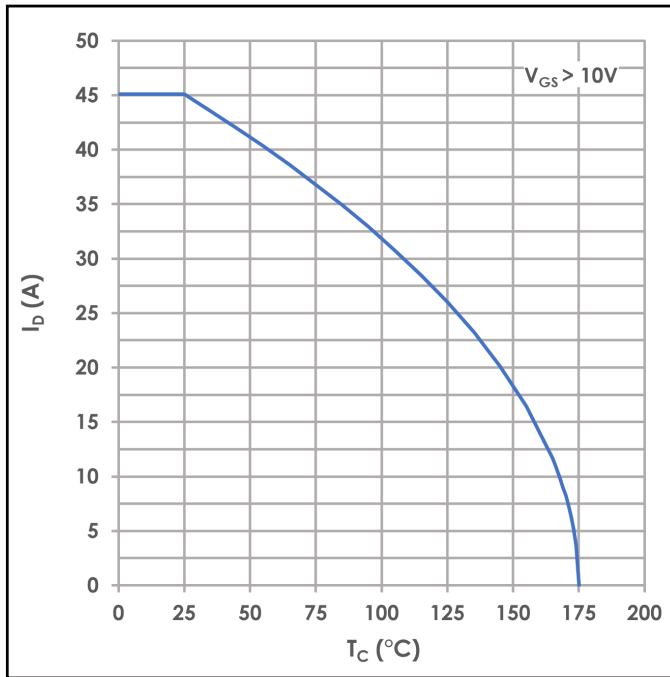


Figure 3: Drain Current

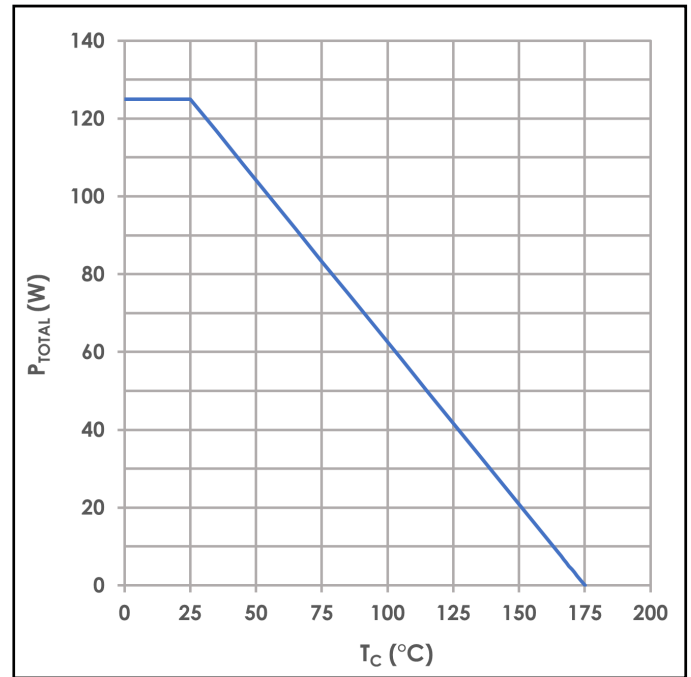


Figure 4: Power Dissipation

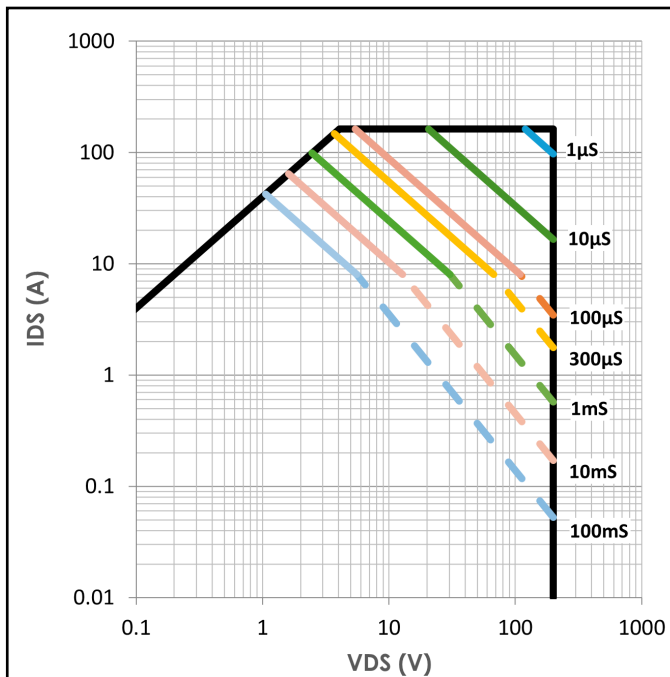


Figure 5: Safe Operating Area

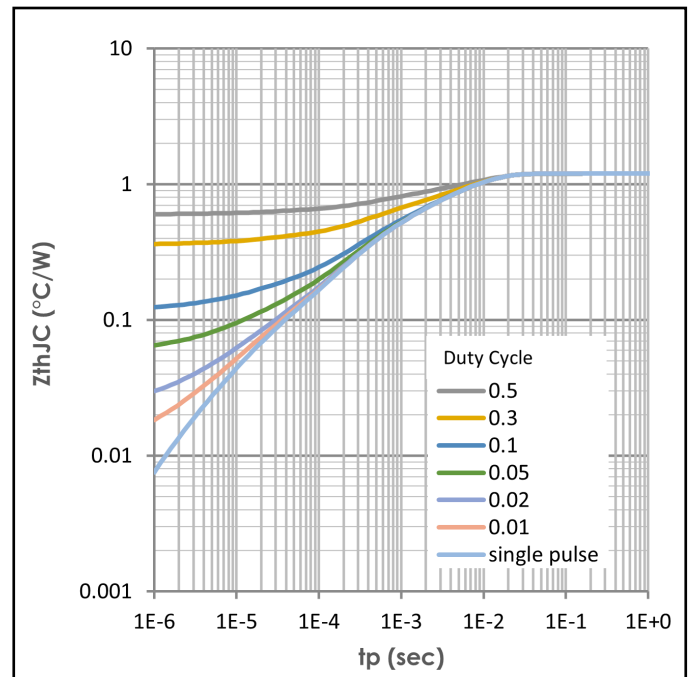


Figure 6: Max Transient Thermal Impedance



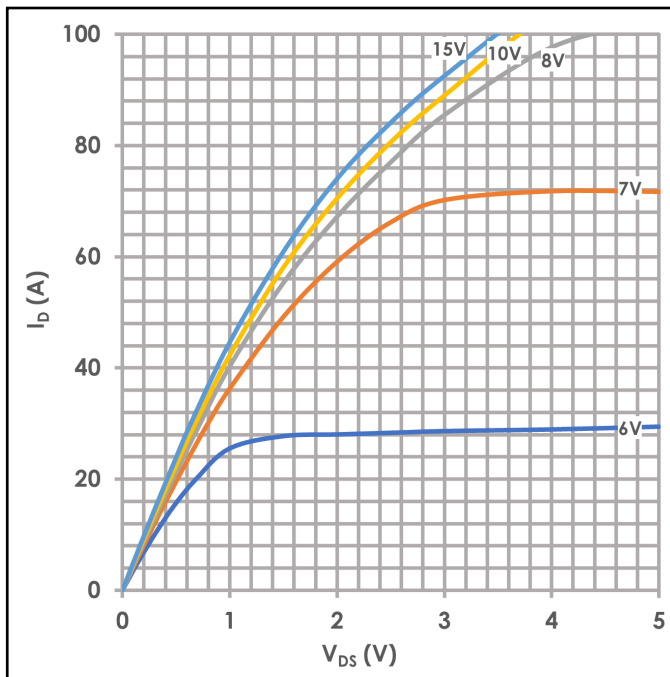


Figure 7: Typical Output Characteristics

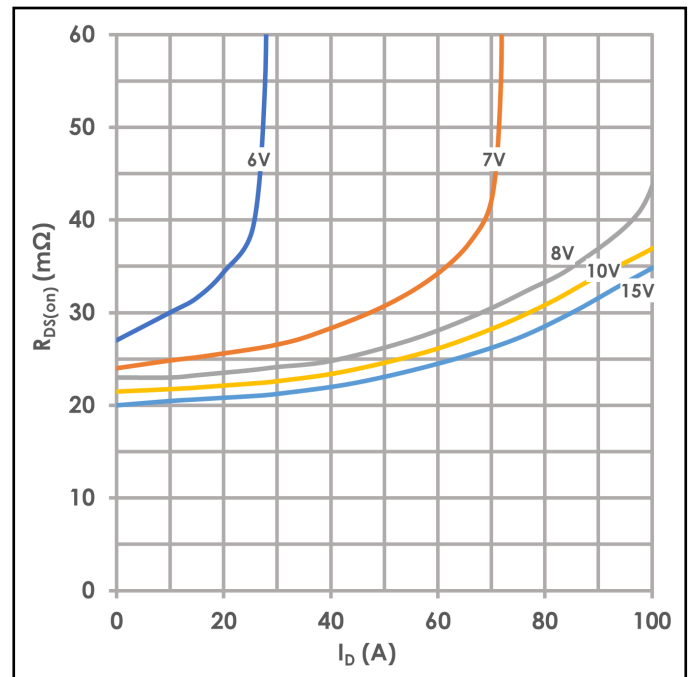


Figure 8: Typical Drain-Source On-Resistance

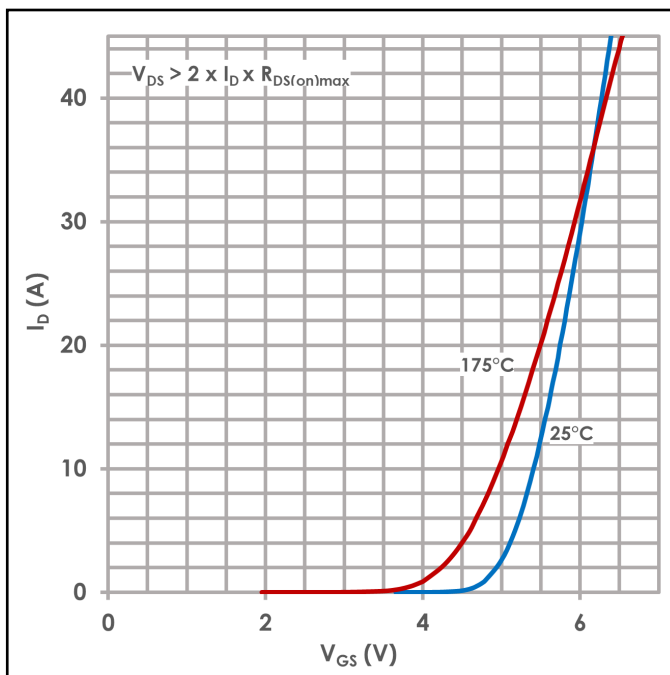


Figure 9: Typical Transfer Characteristics

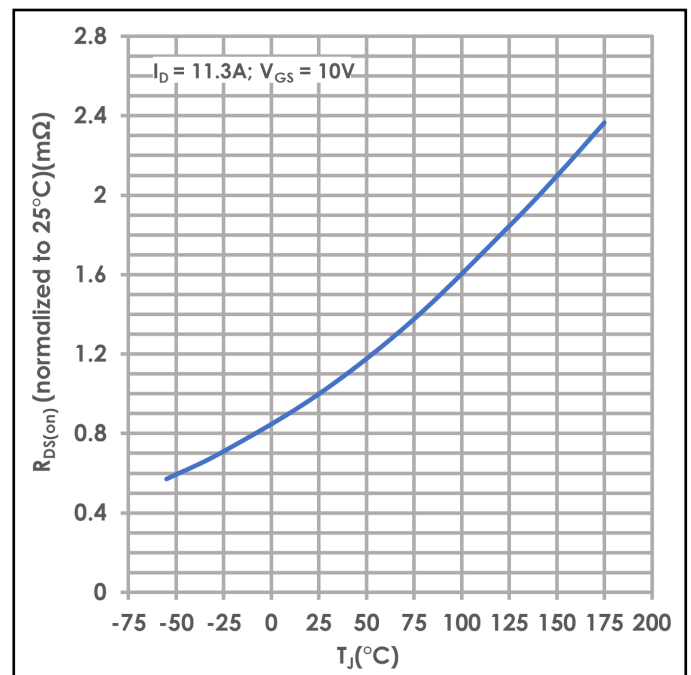


Figure 10: Normalized On-State Resistance vs. Temperature

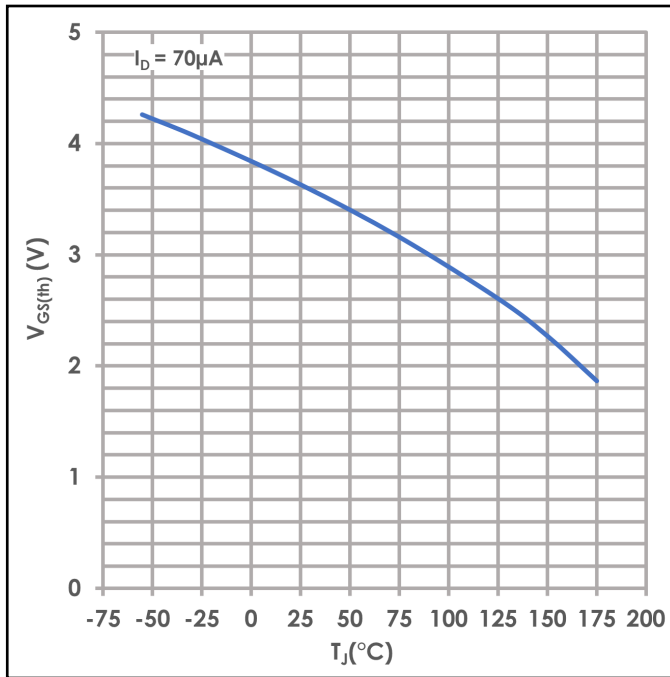


Figure 11: Typical Threshold Voltage

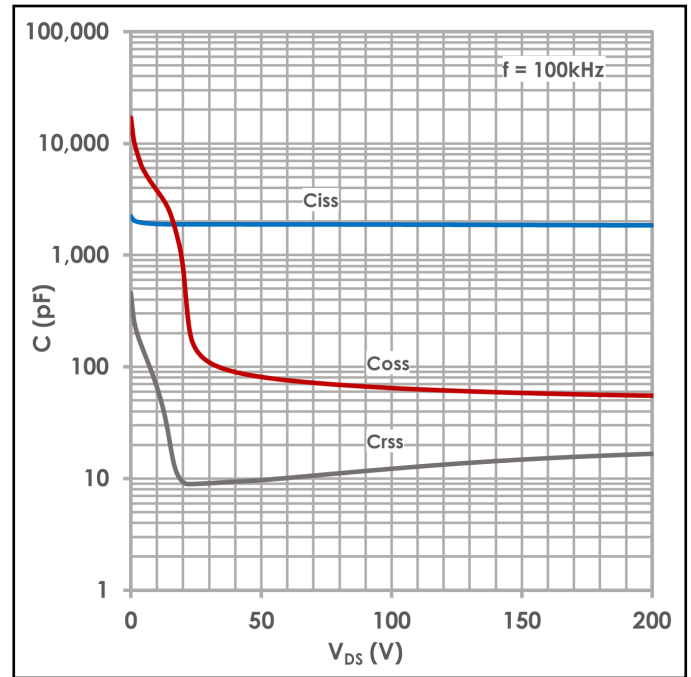


Figure 12: Typical Capacitances

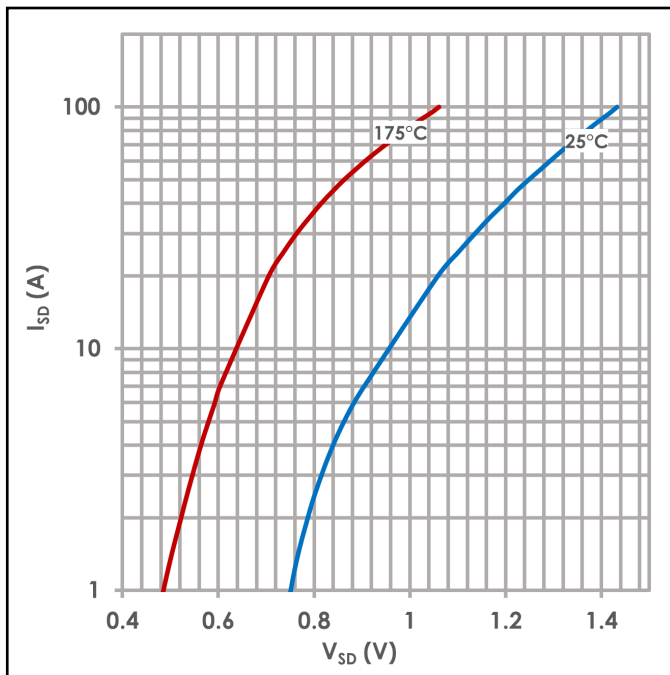


Figure 13: Typical Diode Forward Voltage

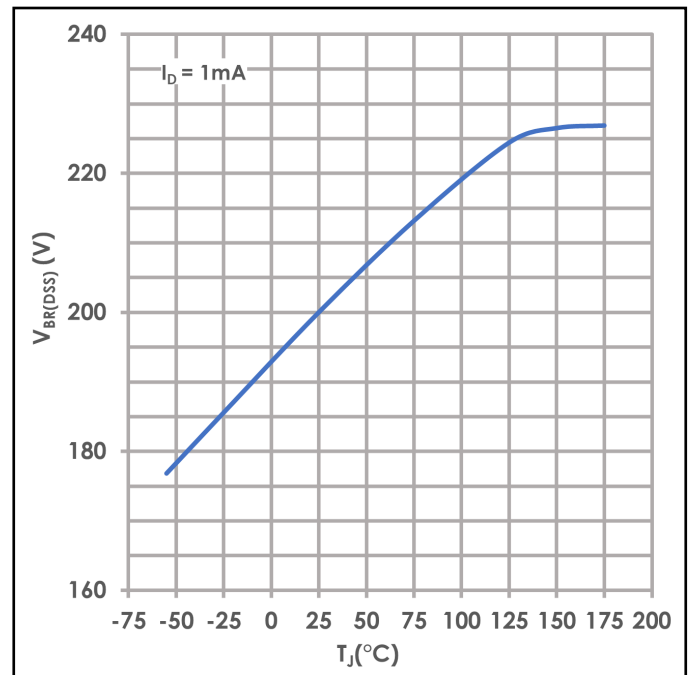


Figure 14: Min Drain-Source Breakdown Voltage

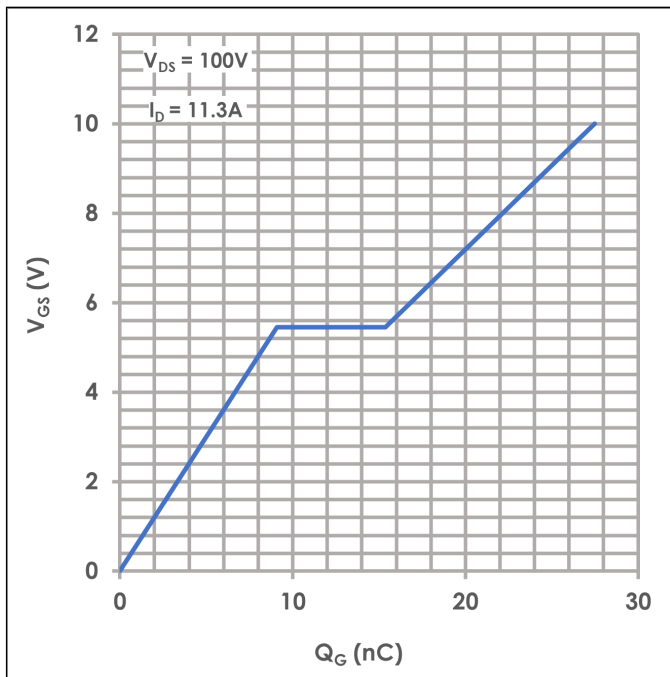


Figure 15: Typical Gate Charge

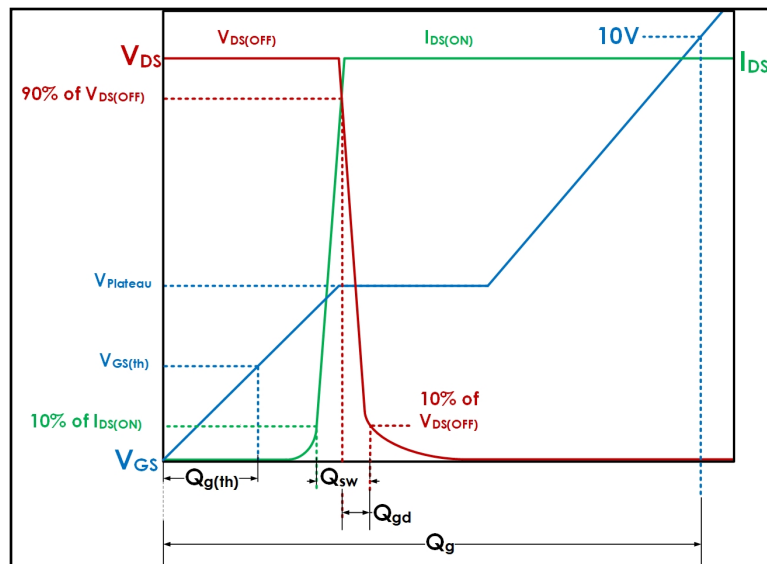
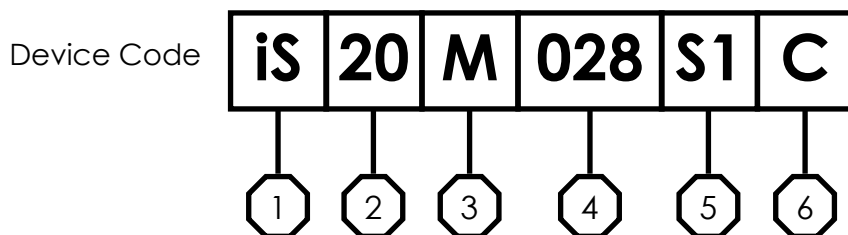








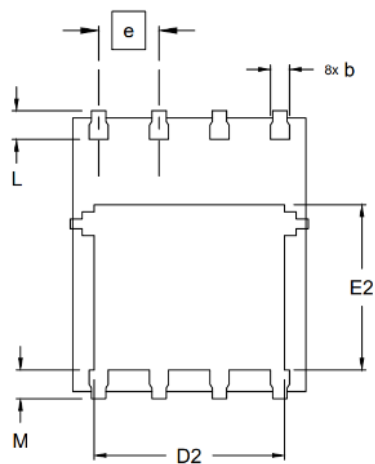
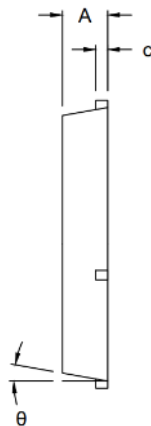
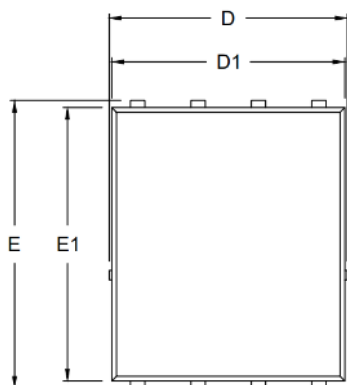
Figure 16: Gate Charge Definitions

DEVICE DECODER RING



-  1 - iDEAL Semiconductor product
-  2 - Voltage rating divided by 10 (200V)
-  3 - M = N-Channel MOSFET, Standard Threshold
-  4 - Maximum drain-to-source resistance
-  5 - SuperQ™ Generation
-  6 - C = PDFN 5x6mm

PDFN 5x6mm Package Drawing



SYMBOL	MIN	MAX
A	0.95	1.05
b	0.31	0.51
c	0.25 REF	
D	4.94	5.30
D1	4.80	5.1
D2	3.70	4.10
E	5.97	6.35
E1	5.67	6.10
E2	3.37	3.76
e	1.27 TYP	
L	0.51	0.71
M	0.51	0.73
θ	0°	10°



Revision History

Version	Date	Comments
1.0	August 2025	Initial Release



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